IS32LT3958 BUCKBOOST EVALUATION BOARD

DESCRIPTION

The IS32LT3958 is a current mode PWM controller designed to drive a low side external NMOS FET for wide input/output voltage range and high LED current applications. An external resistor senses the high side output current of the LED string. A high side sense is the most flexible current sensing scheme, since it functions in either boost or buck-boost mode configurations. The controller can be configured with an external resistor to operate between 100kHz~1MHz frequency resulting in small external inductor and capacitors while maintaining high efficiency. A single capacitor is all that is required to set the spread spectrum dither frequency to reduce the radiated peak emission and optimize the system EMI performance.

The IS32LT3958 integrates circuity to detect output open/short, RT/SYNC pin short, VDD short, VCC under voltage lockout and over temperature fault conditions. These failure conditions can be reported by the open drain fault reporting FAULTB pin. The current monitor pin (IMON) output can be used for continuous LED status check.

The IS32LT3958 can modulate LED current using either analog and/or PWM dimming techniques. The IS32LT3958 features two independent analog dimming pins, ICTRL and ADJR. Input DC voltage in the range of 0.06V~2V on the ICTRL pin and/or ADJR pin is required for analog dimming. PWM dimming is achieved by directly modulating the PWM/EN pin with desired PWM duty cycle or by enabling the internal PWM generator circuit. With the internal PWM generator circuit, IS32LT3958 can achieve stand-alone dual brightness level output. The duty cycle and frequency of the internal PWM generator is easily programmed by the external resistors.

The IS32LT3958 is available in an eTSSOP-20 package with an exposed pad for enhanced thermal dissipation. It operates from 5V to 70V over the temperature range of -40°C to +150°C.

EVALUATION BOARD PHOTO

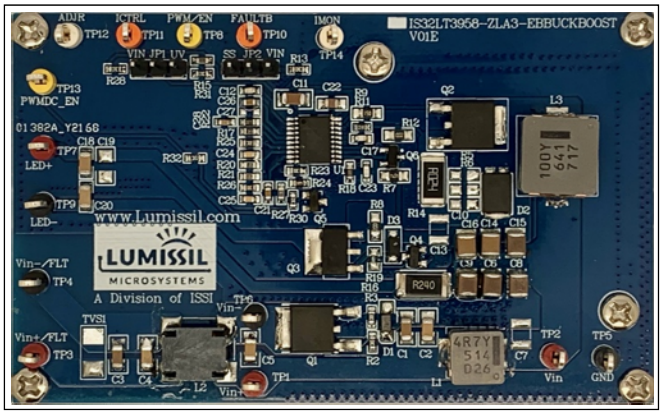

Figure 1 *Photo of IS32LT3958 BUCKBOOST Evaluation Board*

FEATURES

- Wide high voltage input range: 5V to 70V
- Supports boost, buck-boost, SEPIC and buck topology
- Supports either analog, internal PWM dimming or external PWM dimming
- Stand-alone dual brightness output by internal PWM dimming
  - Integrated PWM generator
  - 100Hz~1kHz adjustable PWM frequency
  - 5%~100% adjustable PWM duty cycle
- Excellent analog dimming capability
  - Two analog dimming pins
  - LED binning capability
  - LED over temperature current rolloff
- Externally programmable input undervoltage-lockout
- ±2.8% output current accuracy over -40°C ~ +150°C temperature
- Adjustable operating frequency range of 100kHz~1MHz
- Programmable soft start to avoid inrush current
- EMI reduction capabilities
  - Programmable spread spectrum function
  - Operating frequency synchronization with external clock source
- Fault protection with reporting:
  - VCC under voltage lockout (not reported)
  - Programmable output overvoltage protection
  - Output short circuit protection
  - RT/SYNC pin short protection
  - VDD pin short protection
  - VDD under voltage lockout (not reported)
  - Over temperature protection
- AEC-Q100 Qualified

RECOMMENDED EQUIPMENT

- 9V~16V, 6A DC power supply
- LED load (7~10 LEDs in series/1A)
- Multi-meter

ABSOLUTE MAXIMUM RATINGS

- ≤ 40V power supply

Caution: Do not exceed the conditions listed above, otherwise the board will be damaged.

TEST PROCEDURE

The IS32LT3958 evaluation board is fully assembled and tested. Follow the steps listed below to verify board operation.

Caution: Do not turn on the power supply until all connections are completed.

1) Connect the positive terminal of the power supply to the Vin+/FLT (TP3 terminal) of the board and the negative terminal of the power supply to the Vin-/FLT (TP4 terminal) of the board.
2) Connect the Cathode of the LED load to the LED- (TP9 terminal) of the board. And connect the Anode of the LED load to the LED+ (TP7 terminal) of the board.
3) The jumper JP1 is used to enable/disable the external UVLO function of VCC. If connect JP1 to UV side pin, the PWM/EN pin is connected to VCC via a resistor divider (R15 and R31) on board and the external UVLO function is enabled (typical 7.32V which is programmable by the resistor divider). If connect JP1 to VIN side pin, the PWM/EN pin is pulled up to VCC by R28 on board and the external UVLO function is disabled.
4) If testing external PWM dimming, open the jumper JP1 and apply an external PWM signal to the EN/PWM (TP8 terminal) to achieve external PWM dimming. If external PWM dimming not tested, connect JP1 to VIN side pin and leave the EN/PWM (TP8 terminal) floating and the output PWM will be 100%.

   Note 1: If testing external PWM dimming, please open JP1 to avoid PWM generator damage due to high voltage on the VIN pin.
5) If testing internal PWM dimming, pull the PWMDC_EN (TP13 terminal) high to achieve internal PWM dimming. If internal PWM dimming not tested, leave PWMDC_EN (TP13 terminal) floating and the output PWM will be 100%.
6) If testing analog dimming, apply an external 0.06~2V voltage signal to either ICTRL (TP11 terminal) or ADJR (TP12 terminal) of the board. If analog dimming not tested, leave both ICTRL (TP11 terminal) and ADJR (TP12 terminal) floating and the output will be 100%.
7) The jumper JP2 is used to enable/disable the hiccup mode operation for output overcurrent fault condition. If connect JP2 to VIN side pin, the hiccup mode operation is disabled and the FAULTB pin is pulled up to VCC by R13 on board for the fault reporting. The FAULTB terminal will be pulled low whenever a fault condition is detected. Please refer to table 2 for more details on fault conditions. Connecting JP2 to SS side pin enables the hiccup mode operation.

   Note 2: If the FAULTB pin is connected to an MCU, please remove R13 and pull up by a 10KΩ resistor at the MCU side to avoid MCU damage due to high voltage on the VIN pin.
8) Turn on the power supply and the LED load will light up.
9) To measure the output current, please connect the current meter (multi-meter) in series with the LED load. No matter the power supply voltage or output LED load voltage are changed (in SPEC), the output current of the evaluation board will be always constant.

   Note 3: if the LED load is fixed which means the output power is constant, the power supply current will change following the power supply voltage. The lower power supply voltage the higher power supply current. Please pay attention to the current limit of your power supply, especially at lower power supply voltage.
10) This evaluation board includes an EMI suppression filter circuit and is designed to meet the CISPR-25 conducted EMI standard. To meet class 5 level, the power supply must be connected to Vin+/FLT (TP3 terminal) and Vin-/FLT (TP4 terminal). To save the input common mode chock, connecting the power supply to Vin+ (TP1 terminal) and Vin- (TP6 terminal) still can meet class 4 level.

CAUTION!!! Since the output power is quite high while the DEMO board dimension is compact, the temperature of the components will be quite high. DO NOT touch the components during operation. In practice, some type of heatsinking should to be considered, such as mount a larger heatsink and fill with thermal conductive glue for cooling to ensure thermal reliability.

ORDERING INFORMATION

Part No.	Temperature Range	Package
IS32LT3958-ZLA3-EBBUCKBOOST	-40°C to +125°C (Automotive)	eTSSOP-20, Lead-free

Table 1 *Ordering Information*

For pricing, delivery, and ordering information, please contact Lumissil's analog marketing team at analog@Lumissil.com or (408) 969-6600.

OPERATION FREQUENCY

The internal oscillator of the device is programmable from 100kHz to 1MHz range using a single resistor R_{RT} at RT/SYNC pin. Higher frequency operation results in smaller component size but increases the switching losses and power NMOS gate driving current and may not allow sufficiently high or low duty cycle. Lower frequency gives better performance but results in larger component size. To set a desired frequency, the resistor value can be calculated by following Equation (1):

$$R_{RT} = \frac{2.15\times10^4}{f_{SW}} - 3.7 \qquad (1)$$

Where R_{RT} is in kΩ. f_{SW} is the operation frequency in kHz. In automotive applications, an operation frequency of 400kHz is a good compromise between component size and efficiency. It also makes the system easier to filter switching noise from sensitive frequency bands and pass EMI tests.

If the RT/SYNC pin is connected to an extremely low value resistor or accidently shorted to ground, the internal oscillation frequency will be over 1MHz. If it exceeds 2.5MHz, the internal circuit will detect it and turn off the power NMOS for protection. When this fault condition is removed so the frequency drops below 2.5MHz, the operation will recovery.

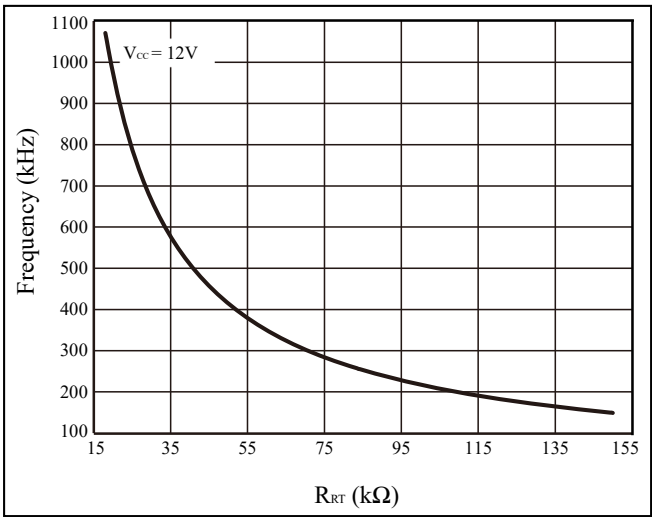

Figure 2 f_{SW} vs. R_{RT}

VCC UVLO

The device features the undervoltage lockout (UVLO) function on VCC pin. It is an internally fixed value which cannot be adjusted. The device is enabled when the VCC voltage rises to exceed V_{UVLO_R}, and disabled when the VCC voltage falls below V_{UVLO_F}.

Besides this internal, fixed UVLO, it may be desirable to externally set a higher UVLO threshold for some applications. A precise UVLO threshold voltage can be set by using a resistor voltage divider between VCC and GND with the center connected to the PWM/EN pin.

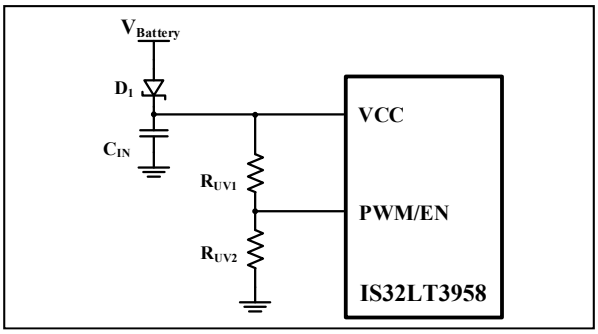

Figure 3 External UVLO for VCC

The external UVLO threshold voltage can be computed by the following Equations:

$$V_{UVLO\_EXTR} = V_{EN\_IH} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \qquad (2)$$

$$V_{UVLO\_EXTF} = V_{EN\_IL} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \qquad (3)$$

The device is enabled when the V_{CC} voltage exceeds V_{UVLO_EXTR}, and disabled when the V_{CC} voltage falls below V_{UVLO_EXTF}.

It is recommended that R_{UV1} and R_{UV2} be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. On the PCB layout, this resistor divider must be placed as close as possible to the PWM/EN pin to avoid noise coupling into the UVLO detection.

LED CURRENT CONTROL

The IS32LT3958 regulates the LED current by the external resistor, R_{IS}, in series with LED string and connecting to ISP and ISN. The internal current sense voltage threshold V_{SENSE}, which is equal to V_{ISP}-V_{ISN}, is 0.25V (Typ.). Since the ISP/ISN only supports high-side current sensing, their common mode voltage (to ground) must be not less than 5V. When the PWM/EN pin is tied to a DC voltage higher than V_{EN_TH}, ICTRL/ADJR voltage is above 2V and PWMDC voltage is above 3V, will result in a full-scale current sense voltage threshold and the LED current can be calculated from following equation (4).

$$I_{LED} = \frac{V_{SENSE}}{R_{IS}} \qquad (4)$$

In order to have an accurate LED current, precision resistors are preferred (±1% recommended). The R_{IS} resistor should be placed as close as possible to the IS32LT3958 device with minimal trace length.

ANALOG DIMMING

The IS32LT3958 offers two analog dimming input pins,

ICTRL and ADJR. The dimming voltage range of both pins is 0.06V to 2V. The current sense voltage threshold, V_{SENSE}, can be regulated by the ICTRL pin and/or ADJR pin voltage. If both analog dimming pins are pulled up above 2V, analog dimming is disabled, and the output current is given by Equation (5). When any one pin is driven below 2V, the analog dimming is enabled, and the pin voltage will proportionally control the current sense voltage threshold V_{SENSE} resulting in a change in the output current as given by following equation:

$$I_{LED\_ADIM} = \frac{V_{ICTRL/ADJR}}{2V} \times \frac{V_{SENSE}}{R_{IS}} \quad (5)$$

If both pins are driven below 2V, the voltage of both pins can control the current sense voltage threshold V_{SNESE} to change the output current:

$$I_{LED\_ADIM} = \frac{(V_{ICTRL} + V_{ADJR}) - 2V}{2V} \times \frac{V_{SENSE}}{R_{IS}} \quad (6)$$

In this equation, if the (V_{ICTRL}+V_{ADJR}) ≤ 2V, the output current will be modulated down close to zero. Due to the GATE minimum on time limitation, the output current will not be completely off. Unless any one of the analog dimming pins is driven below 0.06V (Typ.).

The reference voltage of analog dimming internal circuit is derived from a reference voltage identical with the internal LDO, VDD. Therefore, in the applications, the analog dimming voltage should be derived from the VDD instead of an external voltage source to ensure better accuracy.

EXTERNAL PWM DIMMING

Besides enable and shutdown function, the PWM/EN pin also supports an external PWM signal to implement pulse-width modulation of the output current.

The DIMOUT pin is a buffered output following the dimming signal on the PWM/EN pin which drives the gate of the dimming MOSFET. When the PWM/EN signal voltage is greater than logic high threshold V_{EN_IH}, the switching is enabled and the dimming MOSFET is turned on. When the PWM voltage is lower than the logic low threshold V_{EN_IL}, the switching is disabled and the dimming MOSFET is turned off. The LED string is dimmed by modulating the duty cycle of PWM signal to vary the LED average current. Apply a low PWM signal frequency with a higher device switching frequency will result in best dimming performance. The PWM dimming output current is calculated by:

$$I_{LED\_PWM} = I_{LED} \times D_{EXTPWM} \quad (7)$$

Where, D_{EXTPWM} is the external PWM signal duty cycle in %. The recommended frequency of the external PWM signal is 100Hz~1kHz. There is an inherent PWM turn on/off delay time during continuous PWM dimming.

INTERNAL PWM DIMMING

IS32LT3958 integrates a PWM generator which is controlled by the PWMDC pin. If the PWMDC pin is driven over 3V (Typ.), the internal PWM generator is disabled to get 100% output current which is set by the output current sense resistor, R_{IS}. Once the PWMDC pin is driven below 3V (Typ.), the internal PWM generator is enabled, which drives the switching and the dimming MOSFET to dim the output by its duty cycle. The internal PWM duty cycle is determined by the PWMDC pin voltage:

$$D_{INTPWM} = \frac{V_{PWMDC}}{3V} \times 100 \quad (8)$$

Where, D_{INTPWM} is the internal PWM duty cycle in %.

The recommended internal PWM duty cycle setting range is 5%~100%. The lower duty cycle results in lower output current accuracy due to the error caused by the offset of the internal circuit and the output current rising and falling response time. The PWM dimming output current is calculated by:

$$I_{LED\_PWM} = I_{LED} \times D_{INTPWM} \quad (9)$$

FAULT DETECTION AND REPORTING

For added system reliability, the IS32LT3958 integrates various fault detection and protection circuitry for LED string open/short circuit, VCC and VDD UVLO, power NMOS over current, RT/SYNC and VDD pins short circuit and over temperature conditions. The open drain pin FAULTB can be used as a fault condition flag. When it's monitored by a host, a pull-up resistor from the FAULTB pin to the supply of the host is needed. It is pulled low to report the fault conditions. Table 2 briefly describes the typical protection trigger conditions and device behavior.

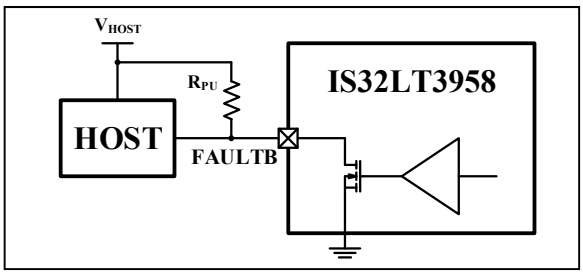

Figure 4 Host Monitors The Fault Reporting

SETTING THE OVER VOLTAGE PROTECTION

The LED string open protection is achieved using overvoltage protection (OVP). The OVP is detected by the OV pin with a resistor divider network from the output to ground. In some cases, when the OV pin voltage reaches the overvoltage protection threshold V_{OVP_TH}, the GATE and DIMOUT pins are immediately pulled low and the FAULTB pin is also pulled low to

report the fault condition. They remain low until the OV pin voltage drops below the hysteresis voltage. To make sure the chip functions properly, the resistor divider (R_{O1}, R_{O2}) at the OV pin should be set to 1.2x greater than the LED string voltage, V_{LED}. For buck-boost applications, since the LED string is referenced to the input, the overvoltage protection should be sensed and translated to ground by using a PNP transistor Q_1 (a signal transistor type).

The OVP voltage (V_{OVP}) is calculated using following equations:

$$V_{OVP} = \frac{V_{OVP\_TH} \times (R_{O1} + R_{O2})}{R_{O2}} \geq 1.2 \times V_{OUT} \qquad (10)$$

The OVP voltage hysteresis is determined by the R_{O1} resistor:

$$V_{OVP\_HY} = I_{OVP\_HY} \times R_{O1} \qquad (11)$$

On the PCB layout, the resistor divider (R_{O1}, R_{O2}) must be placed as close to OV pin as possible. It is recommended to connect a 1nF ceramic capacitor from the OV pin to GND to avoid unexpected noise coupling into this pin when the sensing voltage comes from a long copper trace. This 1nF capacitor should be placed as close to the OV pin as possible.

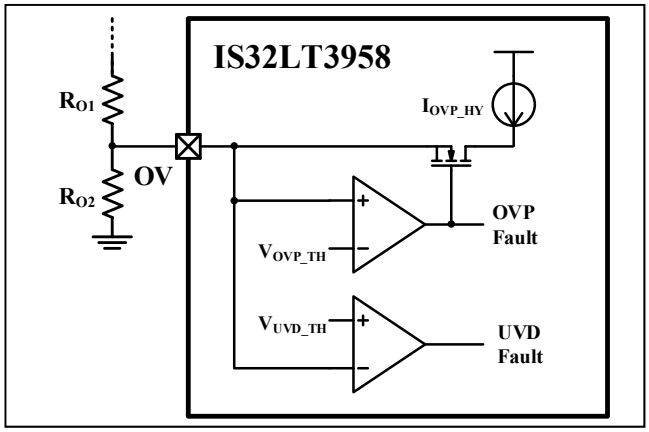

Figure 5 OVP and UVD Circuit

Note, the OVP voltage should not be set much higher than V_{OUT}, otherwise the power NMOS, the dimming MOS, the recirculating diode and the output capacitor would require higher voltage ratings.

Table 2 Fault Actions

Fault Type	Fault Condition	Device Operation After Fault	FAULTB Pin	Fault Reset
VCC UVLO	$V_{CC}<V_{UVLO\_F}$	GATE and DIMOUT pull low immediately. IC enters standby mode. SS and COMP resets to zero.	High Impedance	$V_{CC}>V_{UVLO\_R}$
VDD UVLO	$V_{DD}<V_{UVLO\_F}$	GATE and DIMOUT pull low immediately. IC enters standby mode. SS and COMP resets to zero.	High Impedance	$V_{DD}>V_{UVLO\_R}$
VDD Pin Short	After startup and $V_{DD}<1.4V$	GATE and DIMOUT pulls low immediately. IC enters standby mode. SS and COMP resets to zero.	Pull Low	$V_{DD}>1.4V$
Output Overvoltage (LED Open)	$V_{OV}\geq V_{OVP\_TH}$	GATE and DIMOUT pull low immediately. IC enters standby mode. SS and COMP resets to zero.	Pull Low	$V_{OV}<(V_{OVP\_TH}-V_{OVP\_HY})$
Power NMOS Current Limit	$V_{CS}>V_{CS\_TH}$	GATE pulls low immediately until the next switching cycle.	High Impedance	$V_{CS}<V_{CS\_TH}$
Output Overcurrent (LED Short)	$V_{ISP}/V_{ISN}>5V$ and $(V_{ISP}-V_{ISN})>V_{SENSE\_OC}$	Not internally initiate any protection action and continue to operate. Only if the FAULTB pin is externally connect to SS pin, the device will operate in hiccup mode (restart every t_{SKIP} period).	Pull Low	$(V_{ISP}-V_{ISN})<V_{SENSE\_OC}$
	$V_{ISP}/V_{ISN}<5V$ and $(V_{ISP}-V_{ISN})>V_{SENSE\_OC}$	GATE and DIMOUT pulls low immediately. IC enters standby mode. SS and COMP resets to zero. The device will operate in hiccup mode (restart every t_{SKIP} period).	Pull Low	
Output Undervoltage (LED Short)	$V_{OV}<V_{UVD\_TH}$	Not internally initiate any protection action and continue to operate. Only if the FAULTB pin is externally connect to SS pin, the device will operate in hiccup mode (restart every t_{SKIP} period).	Pull Low	$V_{OV}>V_{UVD\_TH}$
RT/SYNC Pin Short	$f_{SW}>2.5MHz$	GATE pulls low immediately.	Pull Low	$f_{SW}<2.5MHz$
Thermal Shutdown	$T_J>165°C$	GATE and DIMOUT pulls low immediately. IC enters standby mode and SS and COMP resets to zero.	Pull Low	$T_J<150°C$

SCHEMATIC

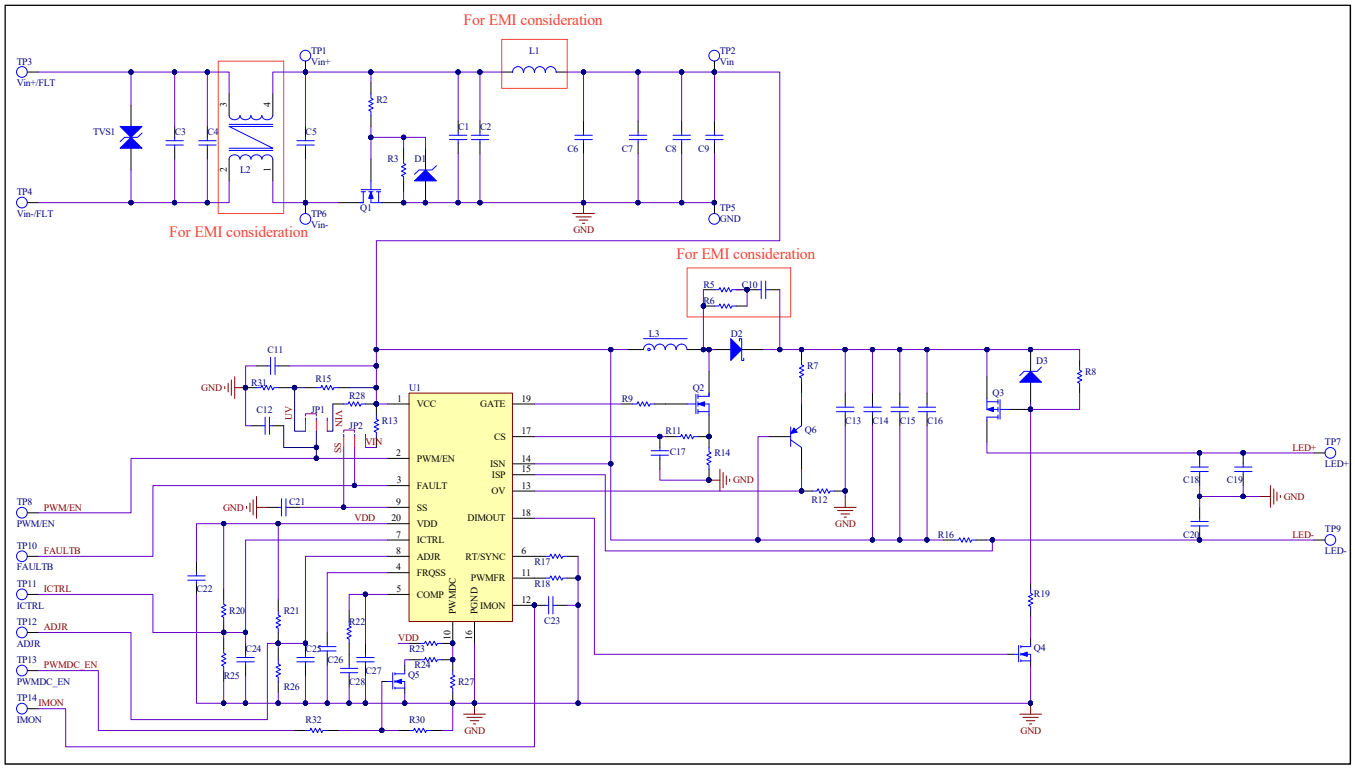

Figure 6 *IS32LT3958 DEMO Schematic*

Note 4: R2, R3, D1 and Q1 form an ideal diode as low loss input reverse polarity protection. They can be replaced by a lower cost Schottky diode, however the much higher forward voltage on Schottky diode will degrade the efficiency and increase thermal on board.

Note 5: The EMI filtering circuits are optional. Using different external components, PCB layout, parameter setting may result in a significantly different EMI performance. Please fine tune EMI filtering circuit based on your actual EMI scan result.

BILL OF MATERIALS

Name	Symbol	Description	Qty	Supplier	Part No.
-	TVS1,R5,R6, C7,C10,C19,C27	NC			
PCB	-	87mm × 53mm, FR-4, 4 layers, 1oz copper	1	-	-
LED Driver	U1	Constant current LED driver	1	Lumissil	IS32LT3958
Capacitor	C1,C3	CAP,2.2μF,50V,±10%,SMD	2	Yageo	AC1206KRX7R9BB225
Capacitor	C2,C4,C5	CAP,0.1μF,50V,±10%,SMD	3	Yageo	AC1206KRX7R9BB104
Capacitor	C6,C8,C9, C14,C15,C16	CAP,10μF,50V,±10%,SMD	6	Murata	GRM32ER71H106KA12L
Capacitor	C11	CAP,1μF,50V,±10%,SMD	1	Yageo	AC1206KRX7R9BB105
Capacitor	C12	CAP,33pF,50V,±10%,SMD	1	Yageo	AC0603KRX7R9BB330
Capacitor	C17,C23	CAP,10pF,50V,±10%,SMD	2	Yageo	AC0603KRX7R9BB100
Capacitor	C18,C20	CAP,22nF,50V,±10%,SMD	2	Yageo	AC0805KRX7R9BB223
Capacitor	C21,C26	CAP,0.1μF,50V,±10%,SMD	2	Yageo	AC0603KRX7R9BB104
Capacitor	C22	CAP,1μF,50V,±10%,SMD	1	Yageo	AC0805KKX7R9BB105
Capacitor	C24,C25	CAP,10nF,50V,±10%,SMD	2	Yageo	AC0603KRX7R9BB103
Capacitor	C28	CAP,220nF,50V,±10%,SMD	1	Yageo	AC0603KKX7R9BB224
Resistor	R2,R13,R28, R30,R31,R32	RES,10k, 0603,±5%,SMD	6	Yageo	AC0603FR-0710KL
Resistor	R3,R23,R25,R26	RES,20k,0603,±5%,SMD	4	Yageo	AC0603FR-0720KL
Resistor	R7	RES,470k, 0805,±5%,SMD	1	Yageo	AC0805FR-07470KL
Resistor	R8	RES,2k, 0805,±5%,SMD	1	Yageo	AC0805FR-072KL
Resistor	R9	RES,15R,0805,±5%,SMD	1	Yageo	AC0805FR-070150L
Resistor	R11	RES,100R, 0603,±5%,SMD	1	Yageo	AC0603FR-07101L
Resistor	R12	RES,10k, 0805,±5%,SMD	1	Yageo	AC0805FR-0710KL
Resistor	R14	RES,0.02R,2512,±1%,SMD	1	UniOhm	25121WF200MT4E
Resistor	R15,R17	RES,51k,0603,±5%,SMD	2	Yageo	AC0603FR-0751KL
Resistor	R16	RES,0.25R,2512,±1%,SMD	1	UniOhm	25121WF250LT4E
Resistor	R18	RES,68k, 0603,±5%,SMD	1	Yageo	AC0603FR-0768KL
Resistor	R19	RES,6.2k, 0805,±5%,SMD	1	Yageo	AC0805FR-076K2L
Resistor	R20,R21,R27	RES,30k, 0603,±5%,SMD	3	Yageo	AC0603FR-0730KL
Resistor	R22	RES,220R, 0603,±5%,SMD	1	Yageo	AC0603FR-07221L
Resistor	R24	RES,6.2k, 0603,±5%,SMD	1	Yageo	AC0603FR-076K2L
MOSFET	Q1,Q2	20A,60V,NMOS	2	DIODES	DMN6040SK3-13
MOSFET	Q3	-3.5A,-60V,PMOS	1	DIODES	ZXMP6A17GTA
MOSFET	Q4,Q5	75mA,60V,NMOS	2	ON	2V7002LT3G
MOSFET	Q6	-200mA,-40V,PNP BJT	1	DIODES	MMBT3906-7-F
Diode	D1,D3	DIODE ZENER 7.5V	2	DIODES	BZT52HC7V5WF-7
Diode	D2	5A,100V	1	DIODES	PDS5100-13

SMD Inductor	L1	4.7μH±20%, I_R=6.3A	1	Panasonic	ETQP5M4R7YFM
SMD Inductor	L2	700Ω@100MHZ, I_R=5A	1	TDK	ACM90V-701-2PL-TL00
SMD Inductor	L3	10μH±20%, I_{SAT}≥7.1A	1	Panasonic	ETQP5M100YFC

PCB LAYOUT (SIZE: 87mm × 53mm, FR-4, 4 LAYERS, 1OZ COPPER)

Note 6: Since the PCB layout is very critical for the EMI performance, please follow this PCB layout's components placement and trace routing for better EMI performance. If need, please contact Lumissil to acquire the PCB layout files/application note for your PCB layout reference.

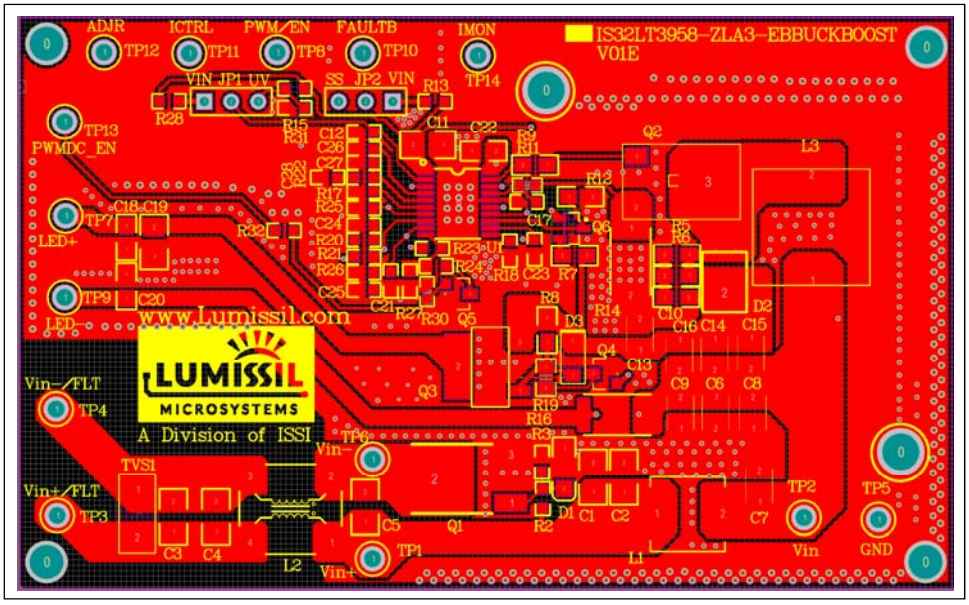

Figure 7 *Board Top Layer*

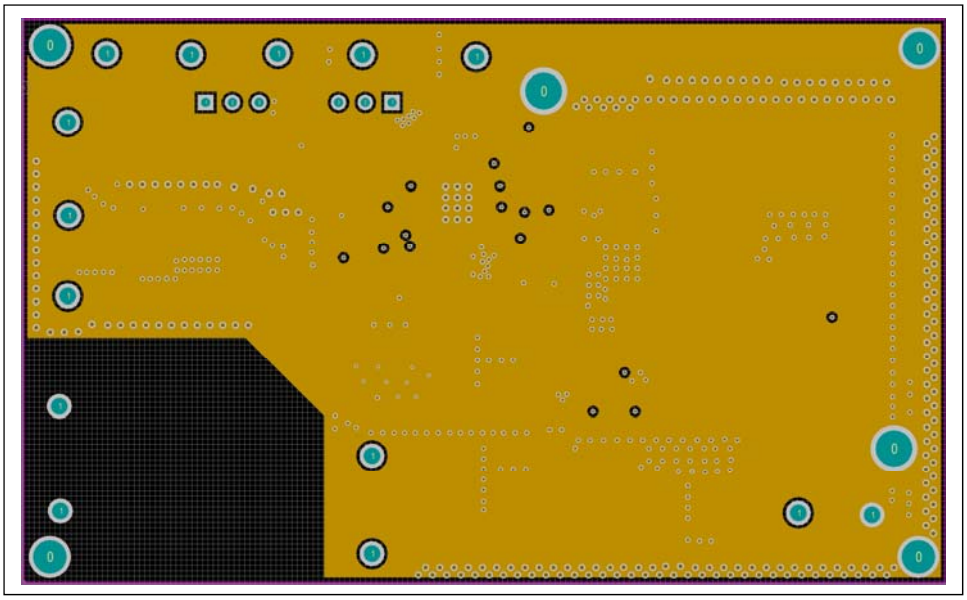

Figure 8 *Board Middle Layer Top*

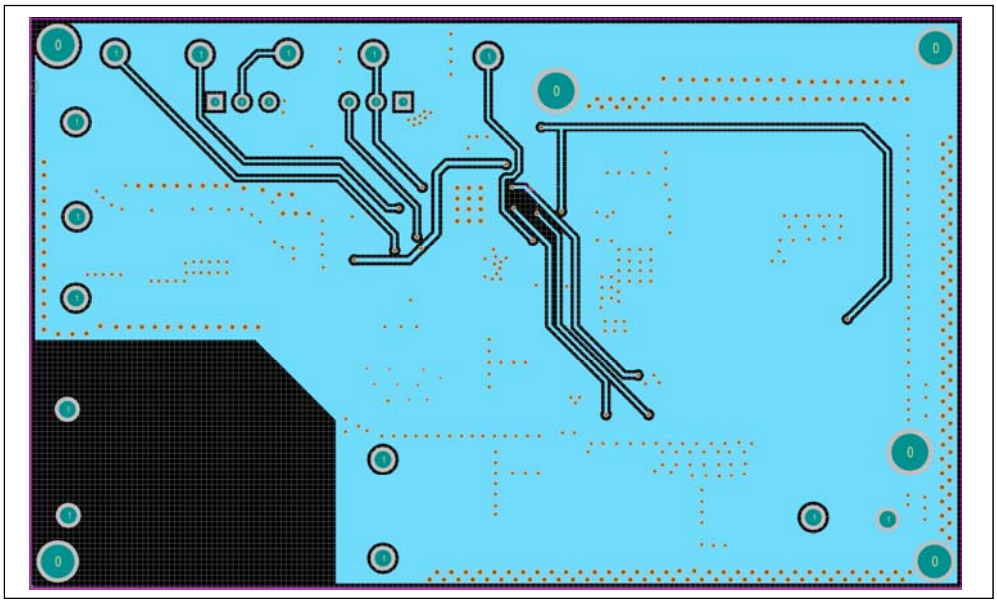

Figure 9 *Board Middle Layer Bottom*

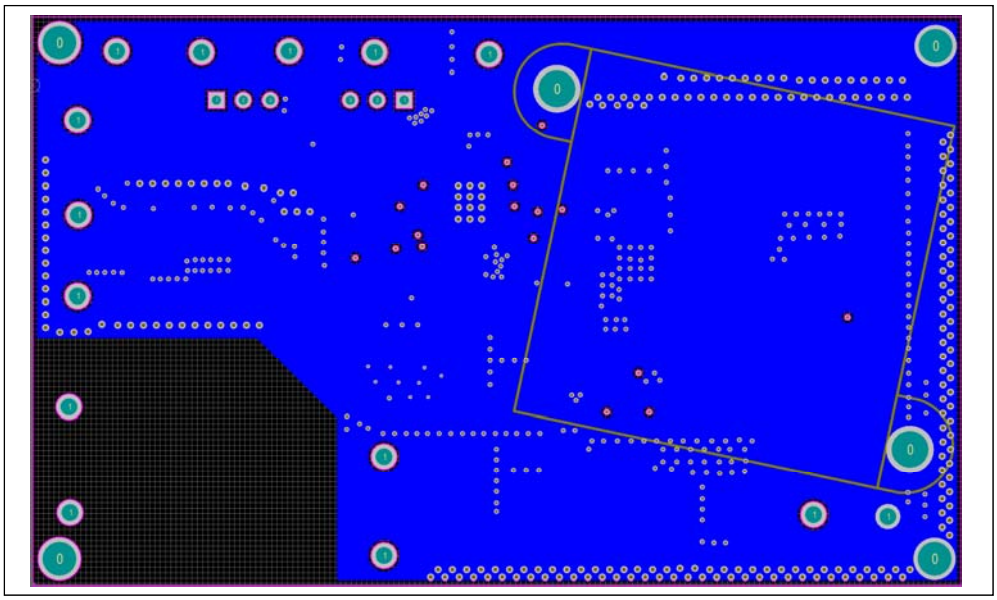

Figure 10 *Board Bottom Layer*

CONDUCTED EMI PERFORMANCE

Test condition: V_{IN}= 12V, V_{LED}= 30V, I_{LED}= 1A, naked board without any shielding

Test standard: CISPR-25 Class 5 and Class 4 conducted EMI (Blue: Peak scanning, Red: Average scanning)

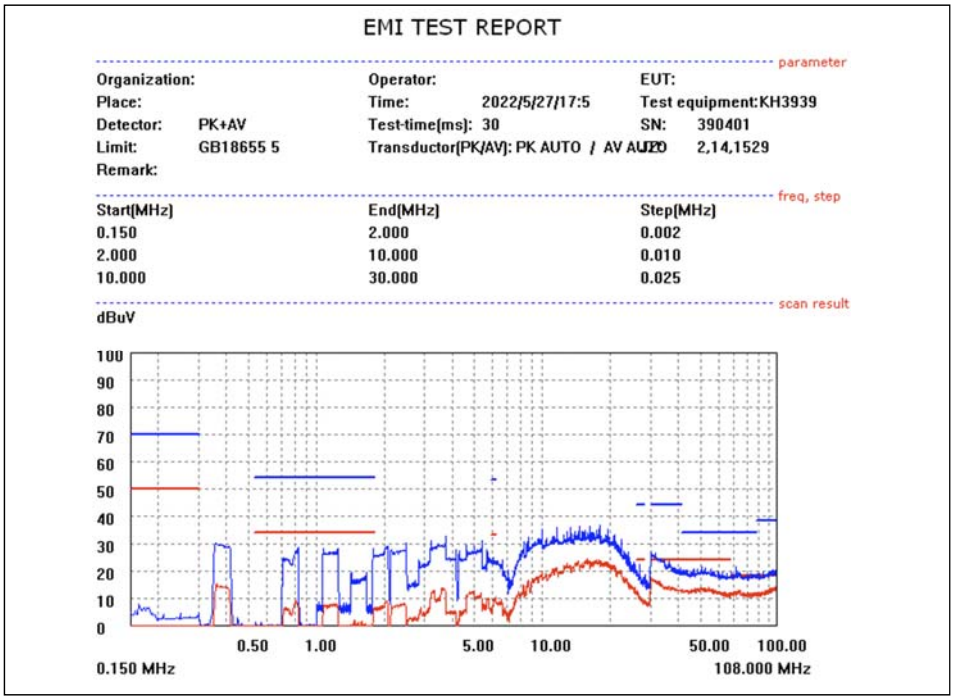

Figure 11 *CISPR-25 Class 5 Conducted EMI Scan (With The Input Common Mode Chock)*

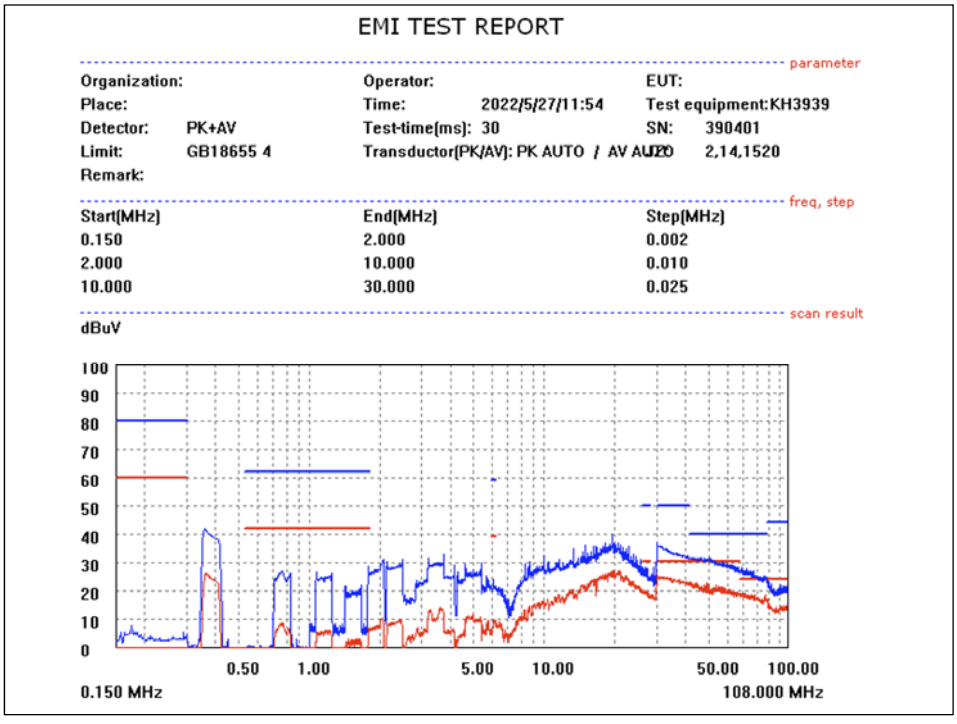

Figure 12 *CISPR-25 Class 4 Conducted EMI Scan (Without The Input Common Mode Chock)*

EFFICIENCY AND LINE REGULATION

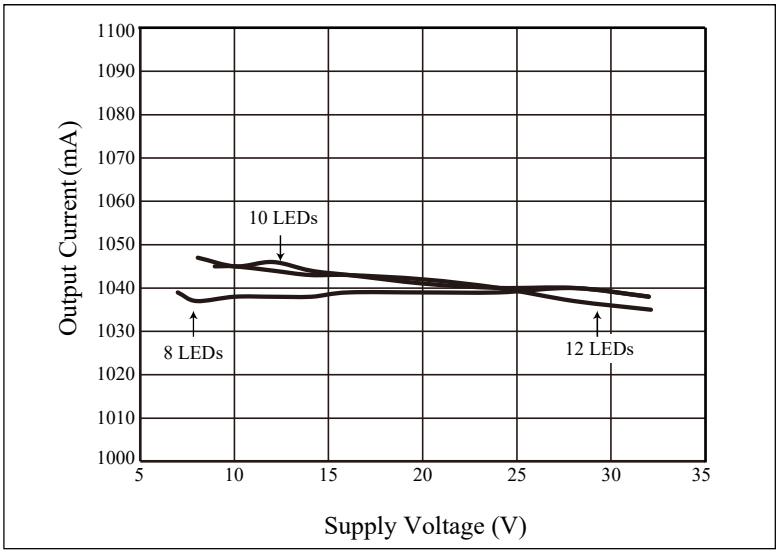

Figure 13 *Line Regulation*

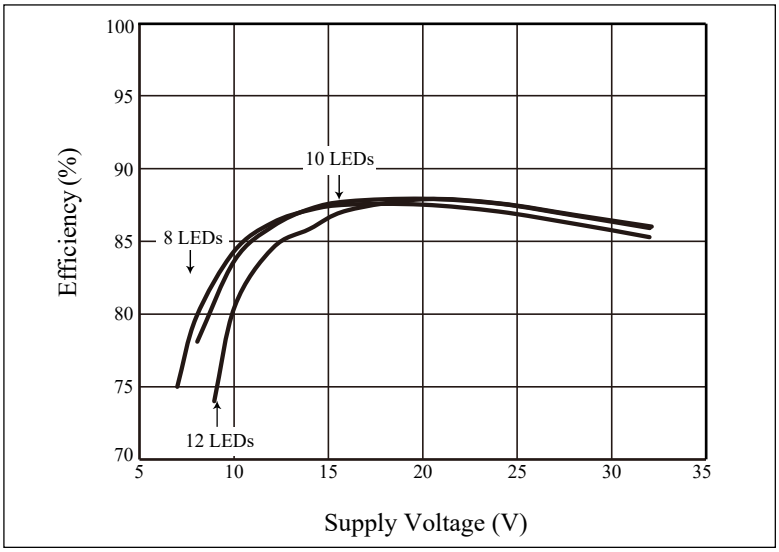

Figure 14 *Efficiency vs. V_{IN}*

REVISION HISTORY

Revision	Detail Information	Data
A	Initial release	2022.08.17