IS32LT3144

THREE-CHANNEL LINEAR LED DRIVER WITH INDIVIDUAL PWM DIMMING AND ANALOG DIMMING

May 2024

GENERAL DESCRIPTION

The IS32LT3144 device is a linear programmable LED driver consisting of three current source output channels capable of up to 150mA each. It supports individual PWM dimming control to each channel. A single resistor sets the maximum current level for all channels. The outputs can be combined to provide a higher current drive capability up to maximum 450mA. A dedicated analog dimming pin can be used for LED binning or in conjunction with an external NTC to implement LED over temperature thermal roll-off protection.

For added system reliability, the IS32LT3144 integrates fault detection circuitry for LED string open/short circuit, single LED short circuit, current setting resistor short, input overvoltage current derating, LED over temperature thermal roll-off, device junction over temperature thermal roll-off and shutdown conditions. Two dedicated fault reporting pins, FAULTB and FAULTS, are able to report fault conditions: the FAULTS pin is dedicated to reporting LED short fault. The fault reporting pins can all be tied together to disable the device and other IS32LT3144 devices on the same parallel circuit to achieve a “one-fail-all-fail” function.

The IS32LT3144 is targeted at the automotive market with end applications to include interior and exterior lighting. For 12V automotive applications the low dropout driver can support one to several LEDs on the output channels. The device is offered in a small thermally enhanced eTSSOP-16 package.

APPLICATIONS

- Rear light
- Stop or taillight
- Position light
- Daytime running light
- Turn Signal Light
- Interior lighting

FEATURES

- Wide input voltage range: 5V~40V
- Three output channels with programmable constant current set by a single resistor
  - 10mA to 150mA per channel
  - ±2%(Typ) current matching by channel (I_{OUTx} >30mA)
  - ±3%(Typ) current accuracy by device (I_{OUTx} >30mA)
  - Combined multiple channels or ICs for higher current capability with same current accuracy
- Low headroom voltage
  - Max. headroom: 500mV at 60mA per channel
  - Max. headroom: 1.1V at 150mA per channel
- Independent PWM dimming per channel
- Analog dimming capability
  - LED over temperature thermal roll-off
  - LED binning
- Fault detection and protection
  - LED string open/short
  - Independent single LED short detection per channel
  - Dedicated fault pin for single LED short fault
  - Current setting resistor short
  - Input overvoltage current derating
  - Junction over temperature thermal roll-off
  - Thermal shutdown
  - Shared fault flag for multiple devices operation to comply with “one-fail-all-fail” function, up to 15 devices
- Operating junction temperature range -40°C to 150°C
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- RoHS & Halogen-Free Compliance
- TSCA Compliance

TYPICAL APPLICATION CIRCUIT

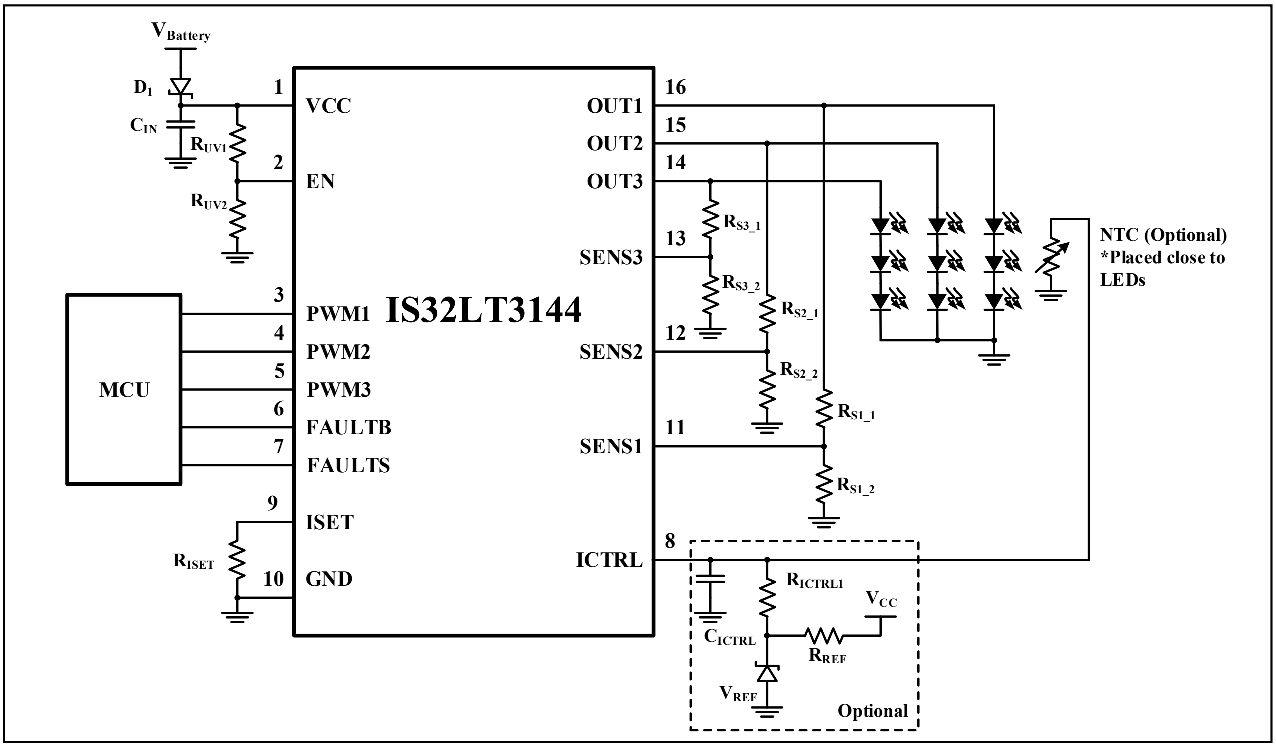
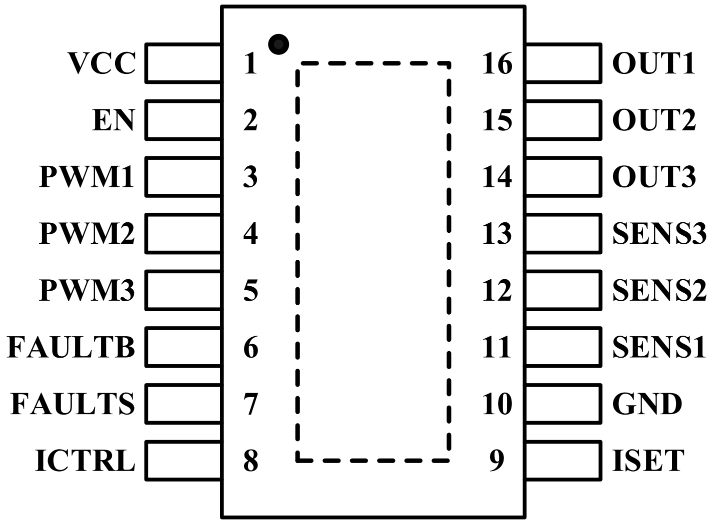


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	VCC	Power supply pin.
2	EN	Enable and shut down pin. It is also used for fault undervoltage lockout (UVLO) voltage threshold setting for LED string open and signal LED short fault detection. If unused, it should be connected to VCC pin.
3~5	PWM1~PWM3	PWM input and channel ON or OFF. Connected to VCC pin if PWM dimming is not used. Connected to GND if the corresponding channel is not used.
6	FAULTB	Fault reporting pin. Active low output driven by the device when it detects a fault condition (except single LED short fault). As an input, this pin will accept an externally generated FAULTB signal to disable the device output to satisfy the "one fail all fail" function. Leave floating if not used.
7	FAULTS	Single LED short fault reporting pin. Active low output driven by the device when it detects a single LED short fault condition. Leave floating if not used.
8	ICTRL	Analog dimming pin. The output is full current when the pin voltage is above 2.3V. Analog dimming is achieved when the pin voltage varies between 0.6V ~ 1.9V. Recommend a 10nF X7R type capacitor close to this pin for noise decoupling. It cannot be left floating. If unused, it can be connected to VCC pin.
9	ISET	Resistor on this pin to GND sets the maximum output current for channel OUT1~OUT3.
10	GND	Ground pin.
11~13	SENS1~SENS3	String voltage sense for single LED short fault detection. Connect to OUTx if not used.
14~16	IOUT3~IOUT1	Current output pin. Connect to SENSx if not used.
	Thermal Pad	Must be connected to GND with sufficient copper plate for heat sink.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY
IS32LT3144-ZLA3-TR IS32LT3144-ZLA3	eTSSOP-16, Lead-free	2500/Reel 96/Tube

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

VCC pin voltage	-0.3V ~ +45V
ISET pin voltage	-0.3V ~ +7V
Other pins voltage	-0.3V ~ V_{CC}-0.3V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Maximum continuous junction temperature, $T_{J(MAX)}$	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JEDEC standard), θ_{JA}	45.4°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JEDEC standard), θ_{JP}	1.617°C/W
Maximum power dissipation, P_{DMAX}	2.75W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J= -40°C ~ +150°C, V_{CC}= 12V, the detail refers to each condition description. Typical values are at T_J= 25°C (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC}	Supply voltage range		5		40	V
V_{UVLO}	VCC undervoltage lockout	Voltage falling		4.1	4.5	V
V_{UVLO_HY}	VCC undervoltage lockout hysteresis			200		mV
I_{CC}	Quiescent current	All PWMx=EN=high, I_{OUTx}= -100mA	2.5	3.5	4.6	mA
I_{SD}	Shutdown current	V_{EN}= 0V			15	μA
I_{CC_FAULT}	Shutdown current in fault mode (from VCC)	PWMx=EN=high, FAULTB=low, V_{CC}= 5V to 40V, I_{OUTx}= -100mA		1.4	2	mA
t_{ON}	Start-up time	V_{CC}> 5V, I_{OUTx}= -60mA, current rises to 50%			200	μs
Current Regulation						
I_{OUTx}	Regulated output current range	Each channel	-150		-10	mA
		Three channels in parallel mode	-450		-30	
I_{OUT_L}	Output current limit per channel	ISET pin grounded		-240		mA
ΔI_{OUT_CH}	Channel-to-channel matching (Note 2)	I_{OUTX}= -10mA, T_J= 25°C	-3		3	%
		I_{OUTX}= -10mA, T_J= -40~125°C	-4		4	
		I_{OUTX}= -30mA, T_J= 25°C	-2		2	
		I_{OUTX}= -30mA, T_J= -40~125°C	-4		4	
		I_{OUTX}= -100mA, T_J= 25°C	-2		2	
		I_{OUTX}= -100mA, T_J= -40~125°C	-3.5		3.5	
		I_{OUTX}= -150mA, T_J= 25°C	-2		2	
		I_{OUTX}= -150mA, T_J= -40~125°C	-3.5		3.5	

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J= -40°C ~ +150°C, V_{CC}= 12V, the detail refers to each condition description. Typical values are at T_J= 25°C (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ΔI_{OUT_DE}	Device accuracy (Note 3)	I_{OUTX}= -10mA, T_J= 25°C	-3.5		3.5	%
		I_{OUTX}= -10mA, T_J= -40~125°C	-6		6	
		I_{OUTX}= -30mA, T_J= 25°C	-3		3	
		I_{OUTX}= -30mA, T_J= -40~125°C	-6		6	
		I_{OUTX}= -100mA, T_J= 25°C	-2.5		2.5	
		I_{OUTX}= -100mA, T_J= -40~125°C	-3.5		3.5	
		I_{OUTX}= -150mA, T_J= 25°C	-2.5		2.5	
		I_{OUTX}= -150mA, T_J= -40~125°C	-3.5		3.5	
V_{ISET_REF}	ISET pin reference voltage			1.15		V
V_{HR_MIN}	Minimum headroom voltage	I_{OUTx}= -150mA per channel		0.65	1.1	
		I_{OUTx}= -60mA per channel		0.26	0.5	
t_{SL}	Current rising slew time	Current rising from 10% to 90% at I_{OUTx}= -60mA	6	12	22	μs
		Current rising from 10% to 90% at I_{OUTx}= -150mA	12	25	45	
	Current falling slew time	Current falling from 90% to 10% at I_{OUTx}= -60mA	10	20	35	
		Current falling from 90% to 10% at I_{OUTx}= -150mA	12	20	35	
EN, PWMx AND ICTRL						
V_{ILEN}	EN pin logic input low level for outputs	OUTx disabled			0.7	V
V_{IHEN}	EN pin logic input high level for outputs	OUTx enabled	2			V
V_{ILEN_FLT}	EN pin input low threshold for LED string open and single LED short detection	Detection disabled		2.49		V
V_{IHEN_FLT}	EN pin input high threshold for LED string open and single LED short detection	Detection enabled	2.5	2.6	2.7	V
V_{HYS_FLT}	EN pin input hysteresis for LED string open and single LED short detection		75	110	145	mV
V_{ILPWM}	PWMx pins input low threshold	OUTx disabled	1.29	1.35	1.41	V
V_{IHPWM}	PWMx pins input high threshold	OUTx enabled	1.34	1.4	1.46	V
V_{HYS_PWM}	PWMx pins input hysteresis			50		mV

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J= -40°C ~ +150°C, V_{CC}= 12V, the detail refers to each condition description. Typical values are at T_J= 25°C (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{DPWM_R}	Delay time between PWM rising edge to 10% of I_{OUTx}	Two LEDs in series		20	45	μs
t_{DPWM_F}	Delay time between PWM falling edge to 90% of I_{OUTx}	Two LEDs in series		20	45	μs
V_{ICTRL}	Analog dimming range		0.6		1.9	V
V_{ICTRL_FU}	Analog dimming fully on threshold		2.3			V
V_{ICTRL_10}	ICTRL pin derates output current by 10%	R_{ISET}= 3.05kΩ		1.75		V
V_{ICTRL_90}	ICTRL pin derates output current by 90%	R_{ISET}= 3.05kΩ		0.59		V
FAULTB Pin						
V_{ILFLTB}	FAULTB logic input low level				0.7	V
V_{IHFLTB}	FAULTB logic input high level		2			V
V_{OLFLT}	FAULTB and FAULTS logic output low level	Tested with 500μA external pull-up			0.7	V
V_{OHFLT}	FAULTB and FAULTS logic output high level	Tested with 1μA external pull-down	2			V
V_{FLT_PU}	FAULTB and FAULTS pin internal pull-up voltage			3.3		V
I_{PD}	FAULTB and FAULTS strong pull-down current	Pulled up to 5V	500	1000	1400	μA
I_{PU}	FAULTB and FAULTS weak pull-up current	Pulled down to ground	3.2	8	17	μA
Protection						
V_{SENS_TH}	SENSx pins detection voltage threshold	V_{EN}> V_{IHEN_FLT}	1.34	1.4	1.46	V
I_{LKG}	SENSx pins leakage current	V_{SENSx}= 3V			500	nA
t_{SENS}	Single LED short circuit detection deglitch		1	2	3	ms
		During PWM dimming, count the number of continuous cycles when V_{SENSx}< V_{SENS_TH}	7		8	Cycles
V_{OVTH}	VCC overvoltage threshold	Output current derates by 10%	19.2	20.6	22	V
V_{OVRG}	VCC overvoltage derating range	Output current derates from 90% to 60%		1.6		V
V_{OCD}	LED string open detection voltage	(V_{CC} - V_{OUTx}) voltage falling and V_{EN}> V_{IHEN_FLT}	50	116	180	mV
V_{OCD_HYS}	LED string open detection hysteresis	(V_{CC} - V_{OUTx}) voltage rising and V_{EN}> V_{IHEN_FLT}	90	180	300	mV

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J= -40°C ~ +150°C, V_{CC}= 12V, the detail refers to each condition description. Typical values are at T_J= 25°C (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{OCD}	LED string open detection deglitch		1	2	3	ms
		During PWM dimming, count the number of continuous cycles when (V_{CC} - V_{OUTx}) < V_{OCD}	7		8	Cycles
V_{SCD}	LED string short detection voltage	Measured at OUTx pin, voltage falling	0.7	0.78	0.86	V
V_{SCD_HYS}	LED string short detection voltage hysteresis		120	200	280	mV
I_{RTR}	Fault retry current		3	5	7	mA
t_{SCD}	LED string short detection deglitch		1	2	3	ms
		During PWM dimming, count the number of continuous cycles when V_{OUTx}< V_{SCD}	7		8	Cycles
R_{ISET_SC}	ISET pin resistor short detection	FAULTB goes low	1.55	1.89	2.3	kΩ
Thermal Monitor						
T_{SD}	Thermal shutdown	(Note 4)		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 4)		15		°C
T_{RO}	Thermal roll-off activation temperature	90% of I_{OUTx} (Note 4)		153		°C
I_{RO_ISR}	Thermal roll-off current derating slew rate	(Note 4)		3.5		%/°C
I_{RO_IMIN}	Thermal roll-off minimum current	(Note 4)		20		%

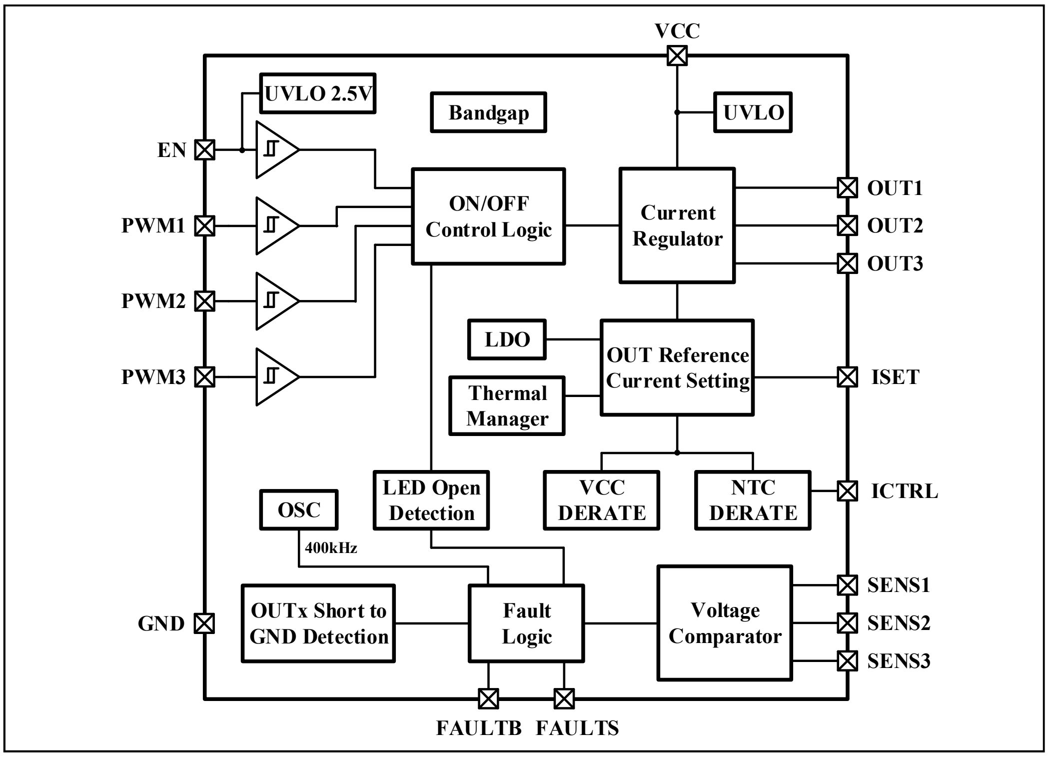
Note 2: I_{AVG}= (I_{OUT1} + I_{OUT2} + I_{OUT3})/3, ΔI_{OUT_CH}= (I_{OUTx}-I_{AVG})/I_{AVG}

Note 3: $I_{SETTING}$ is the target current set by R_{ISET}. ΔI_{OUT_DE}= (I_{OUTx}-$I_{SETTING}$)/$I_{SETTING}$

Note 4: Guaranteed by design.

Note 5: Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

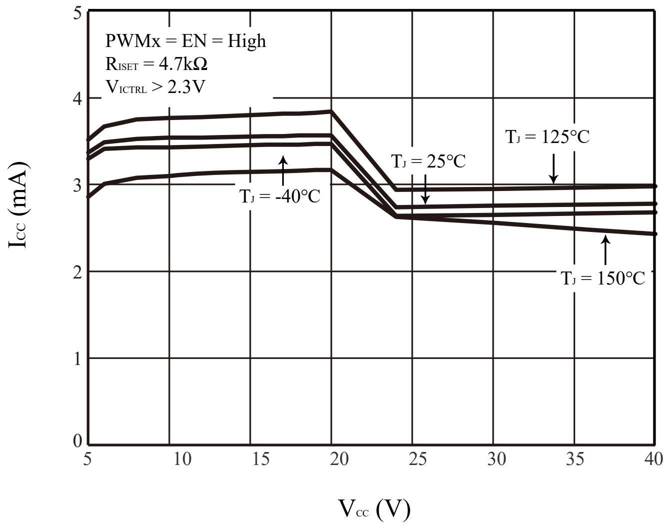


Figure 2 I_{CC} vs. V_{CC}

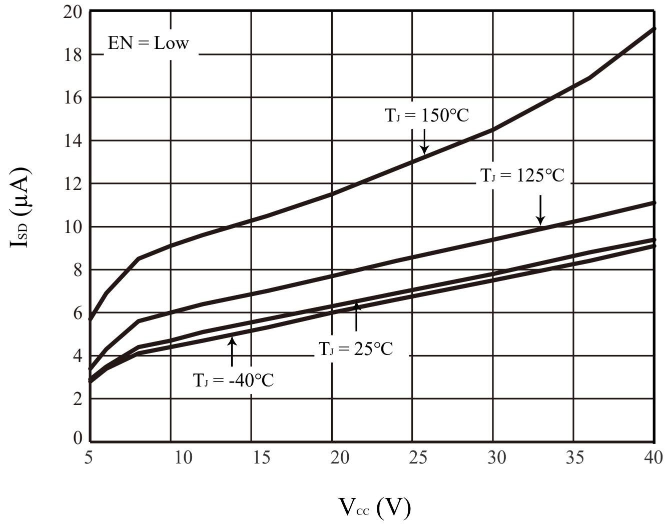


Figure 3 I_{SD} vs. V_{CC}

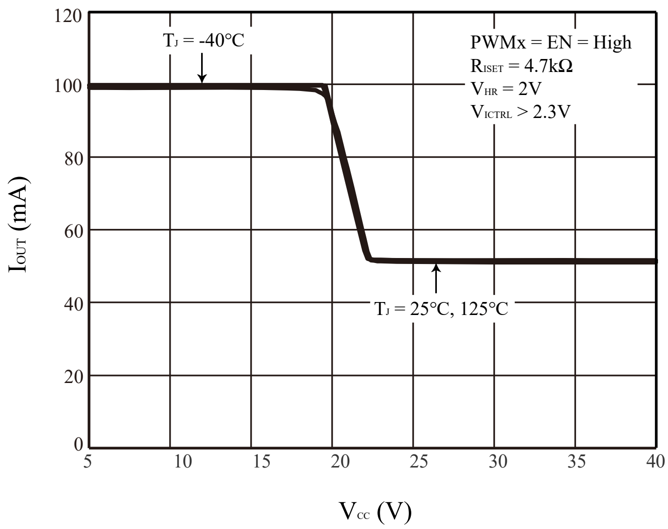


Figure 4 I_{OUT} vs. V_{CC}

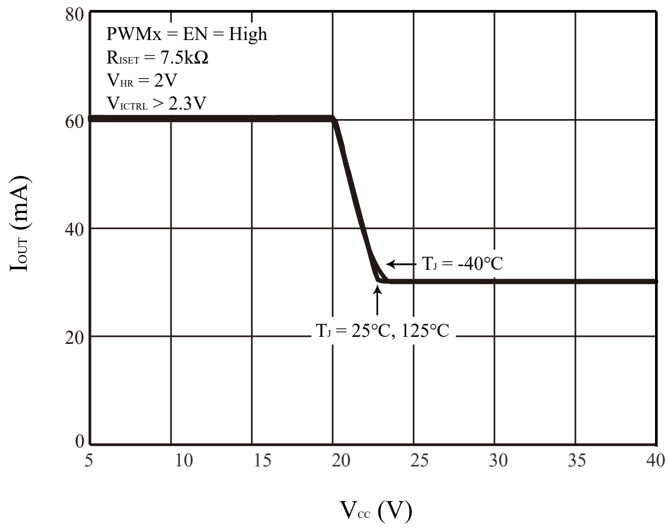


Figure 5 I_{OUT} vs. V_{CC}

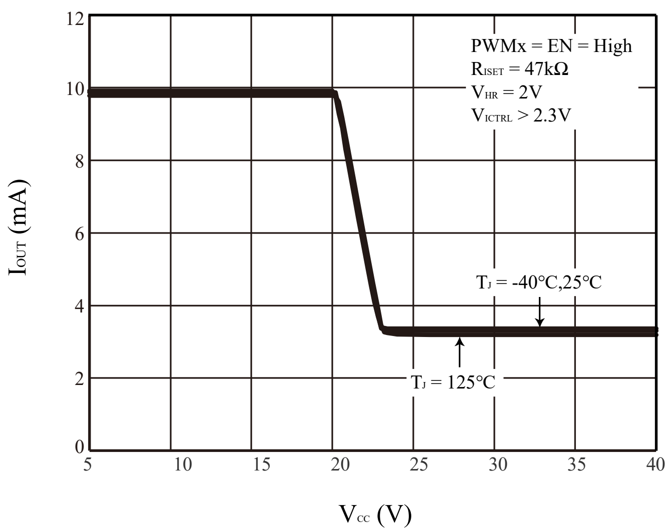


Figure 6 I_{OUT} vs. V_{CC}

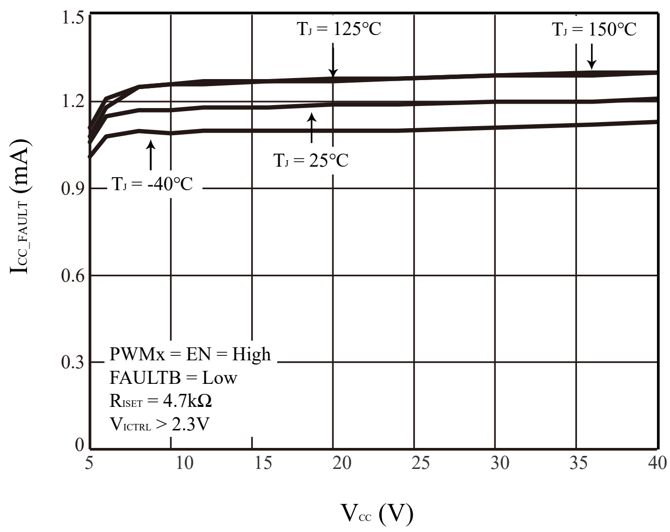


Figure 7 I_{CC_FAULT} vs. V_{CC}

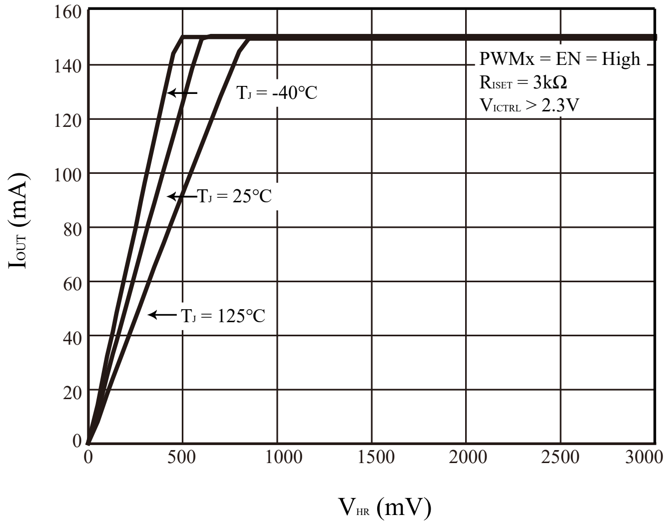


Figure 8 I_{OUT} vs. V_{HR}

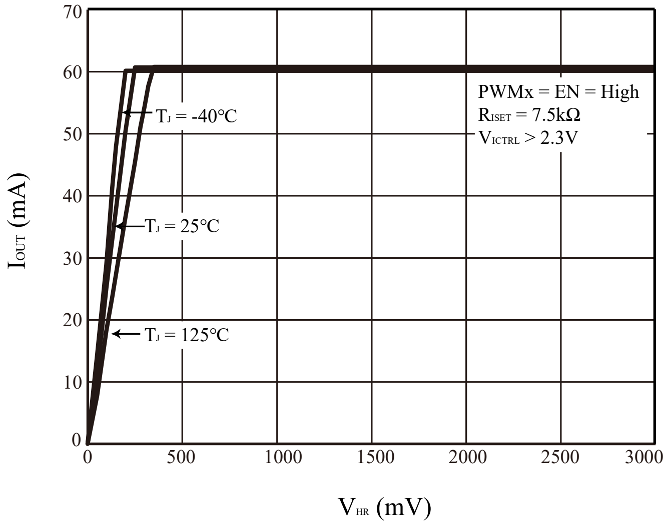


Figure 9 I_{OUT} vs. V_{HR}

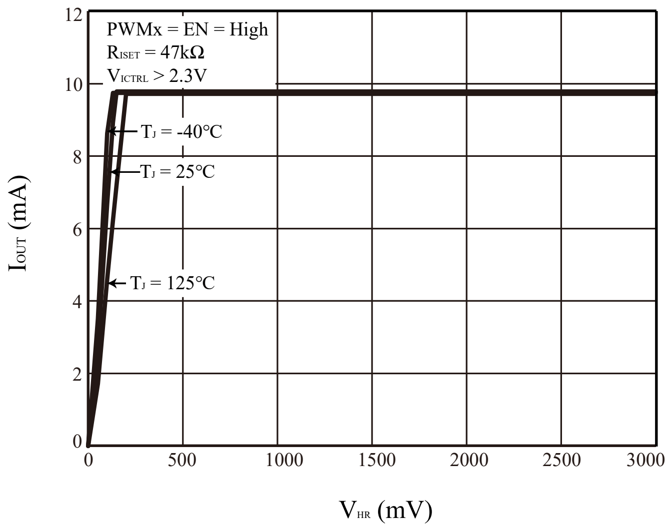


Figure 10 I_{OUT} vs. V_{HR}

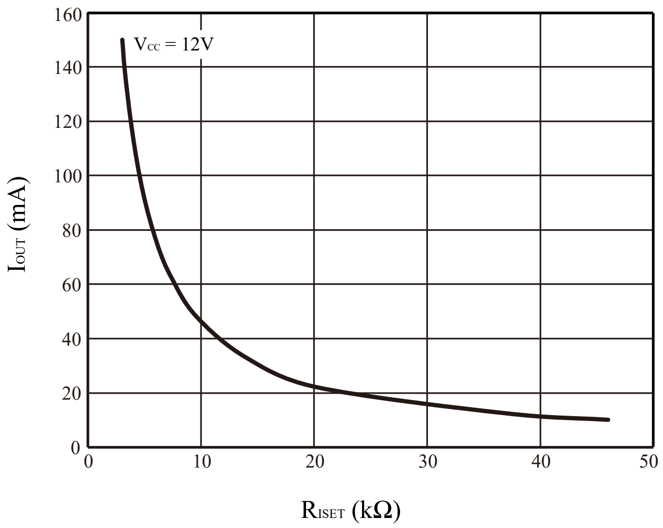


Figure 11 I_{OUT} vs. R_{ISET}

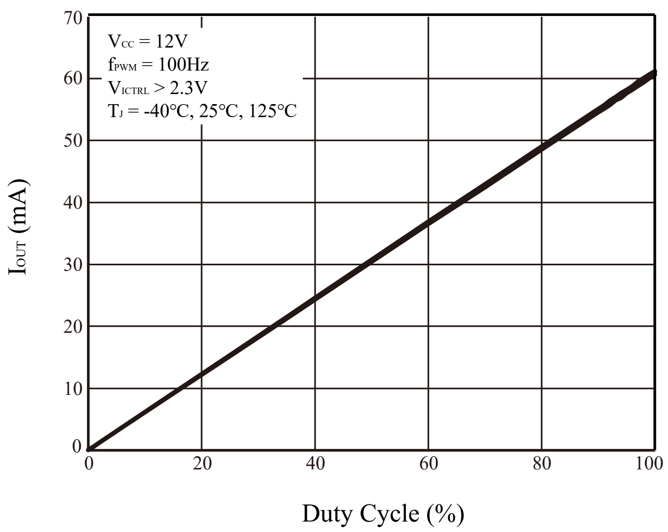


Figure 12 I_{OUT} vs. Duty Cycle

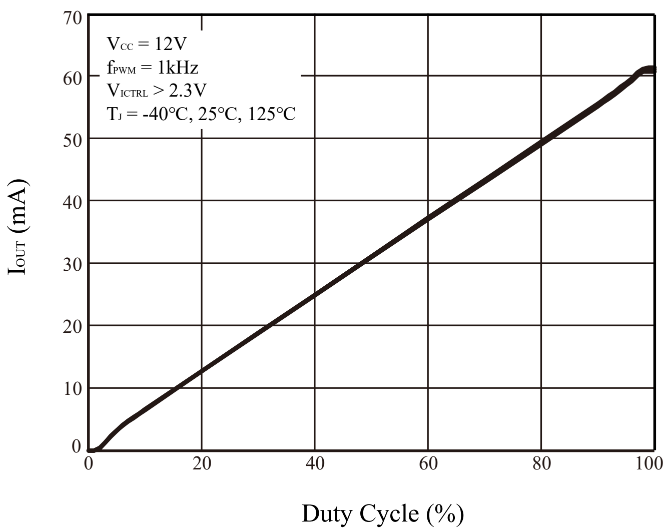


Figure 13 I_{OUT} vs. Duty Cycle

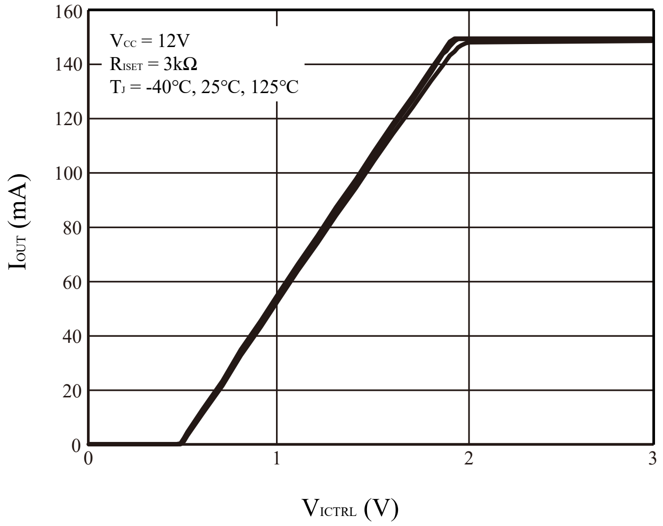


Figure 14 I_{OUT} vs. V_{ICTRL}

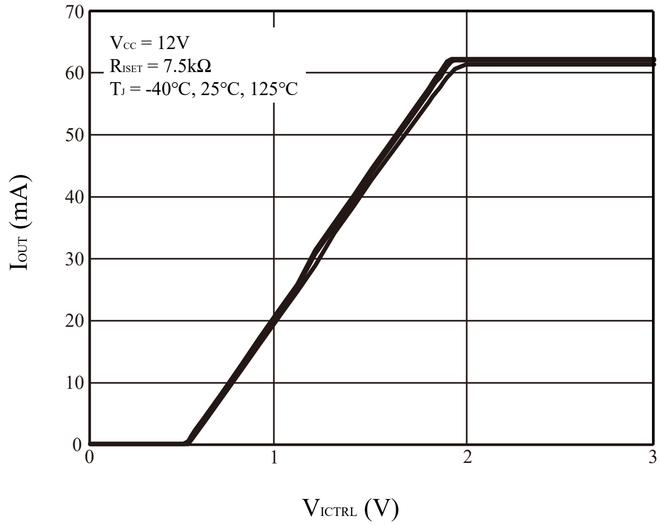


Figure 15 I_{OUT} vs. V_{ICTRL}

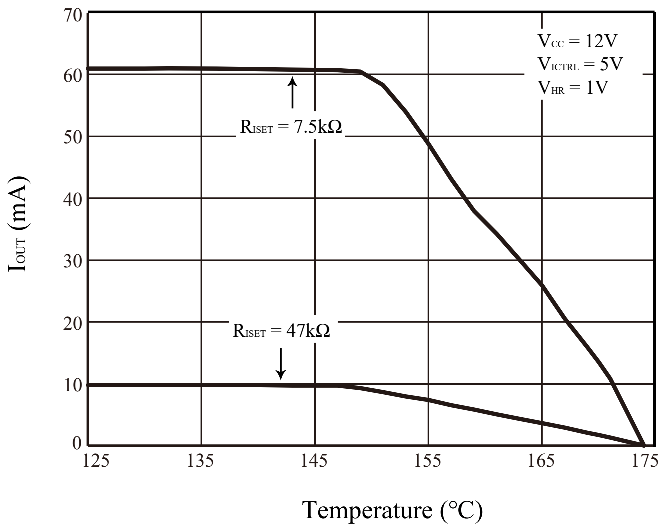


Figure 16 I_{OUT} vs. Temperature (Thermal Roll-Off)

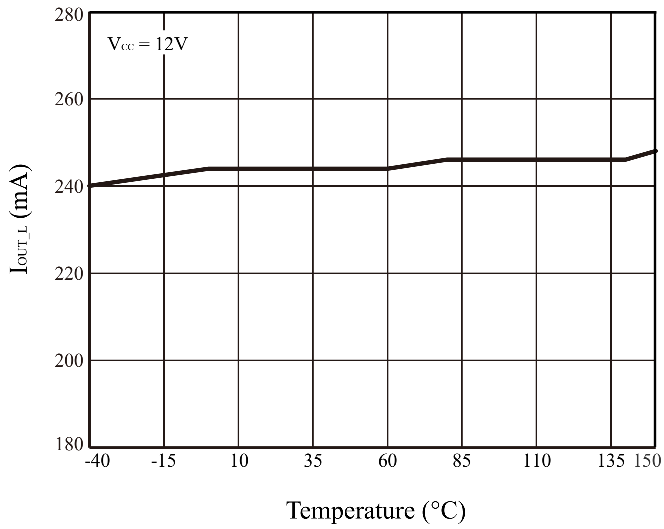


Figure 17 I_{OUT_L} vs. Temperature

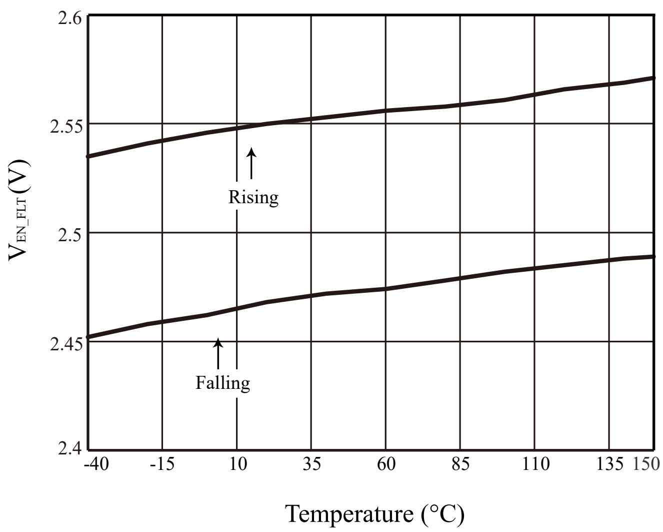


Figure 18 V_{EN_FLT} vs. Temperature

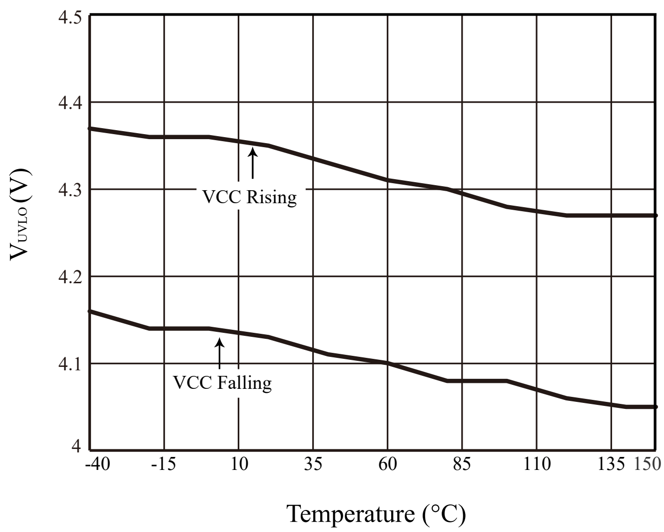


Figure 19 V_{UVLO} vs. Temperature

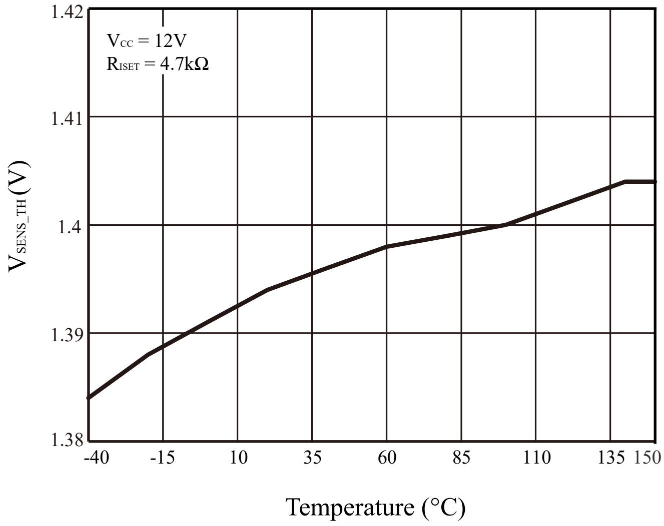


Figure 20 V_{SENS_TH} vs. Temperature

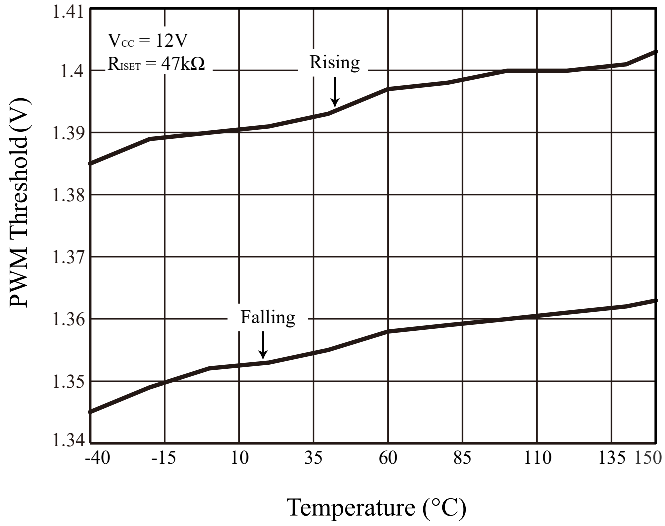


Figure 21 PWM Threshold vs. Temperature

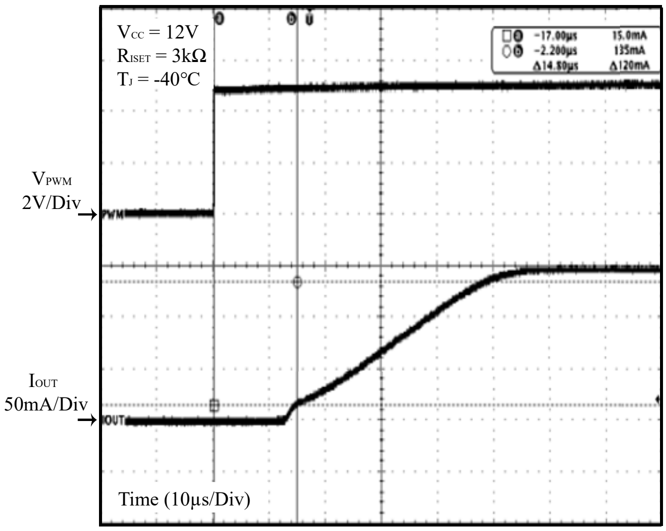


Figure 22 PWM On

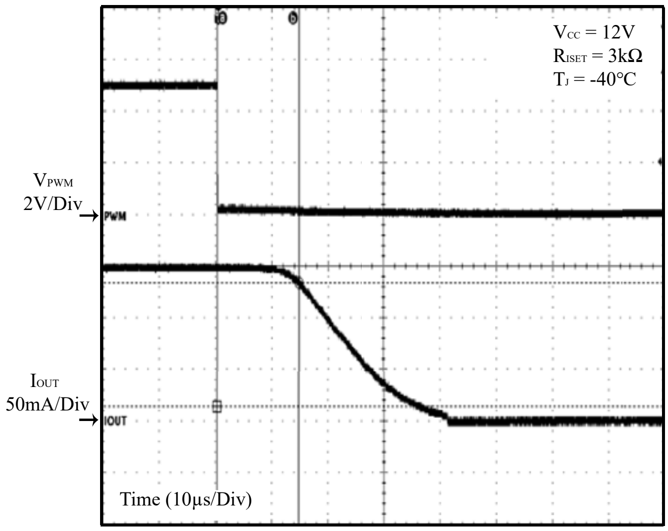


Figure 23 PWM Off

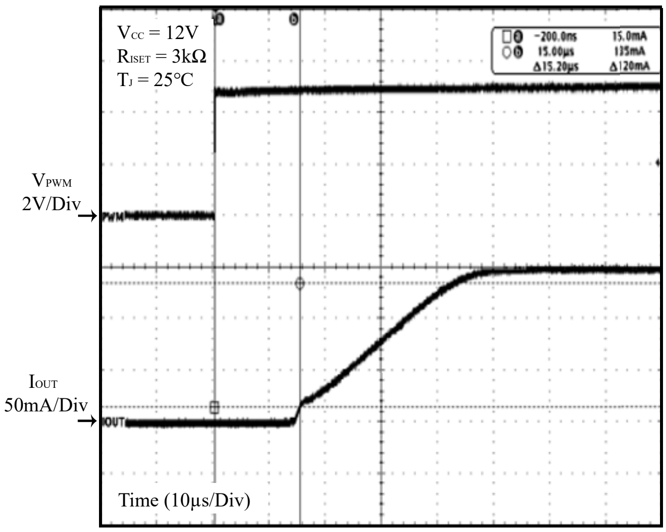


Figure 24 PWM On

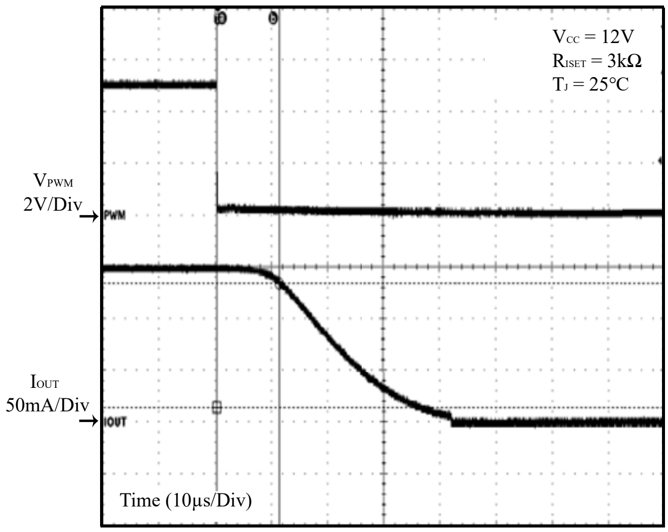


Figure 25 PWM Off

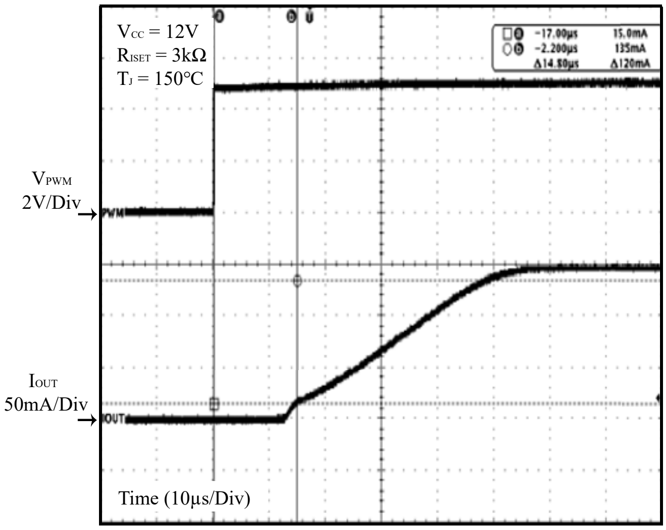


Figure 26 PWM On

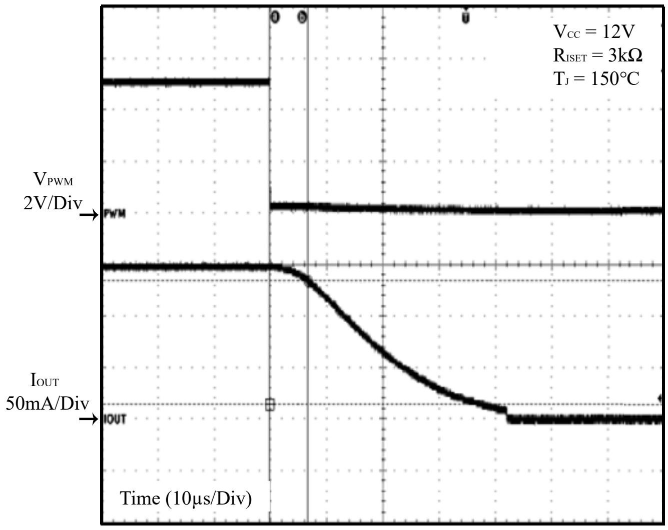


Figure 27 PWM Off

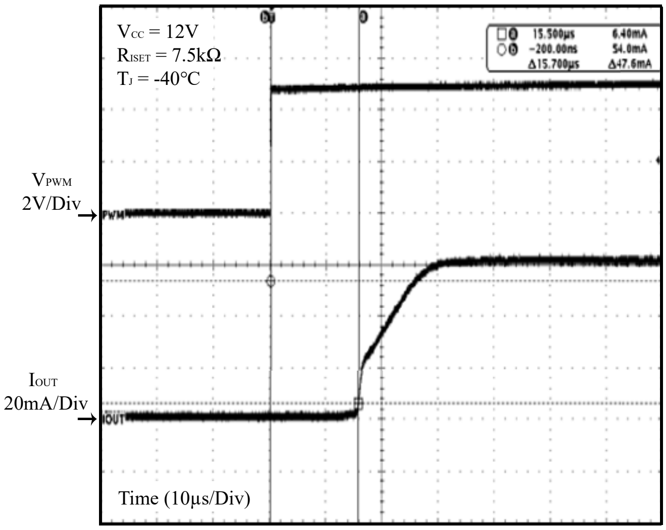


Figure 28 PWM On

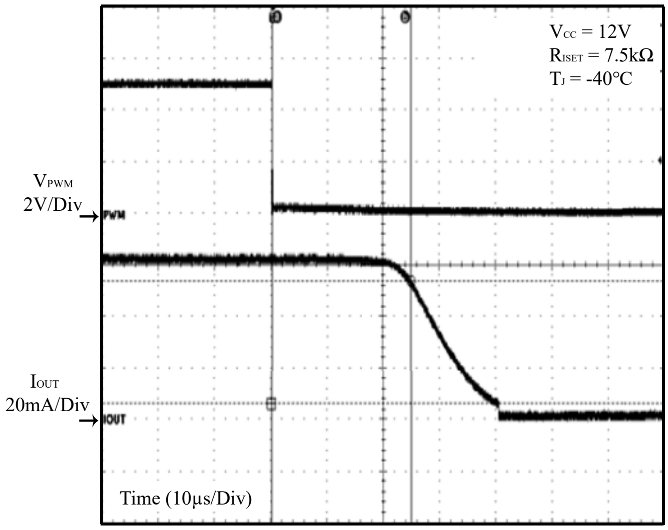


Figure 29 PWM Off

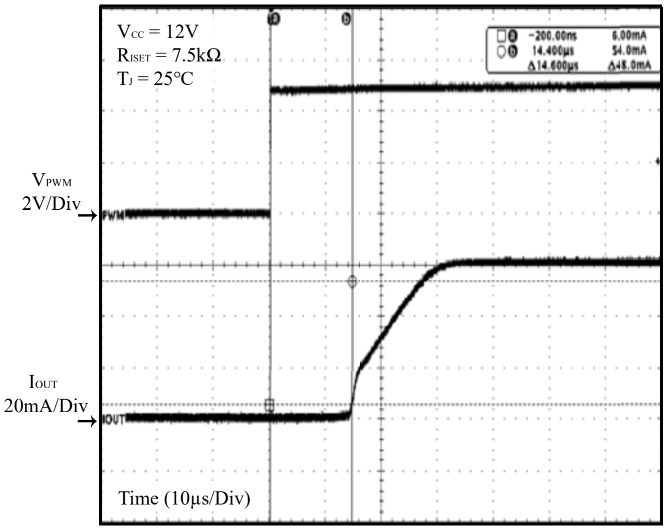


Figure 30 PWM On

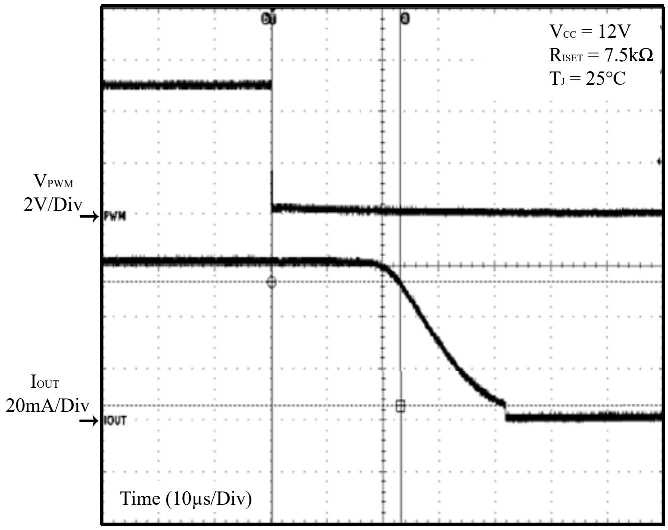


Figure 31 PWM Off

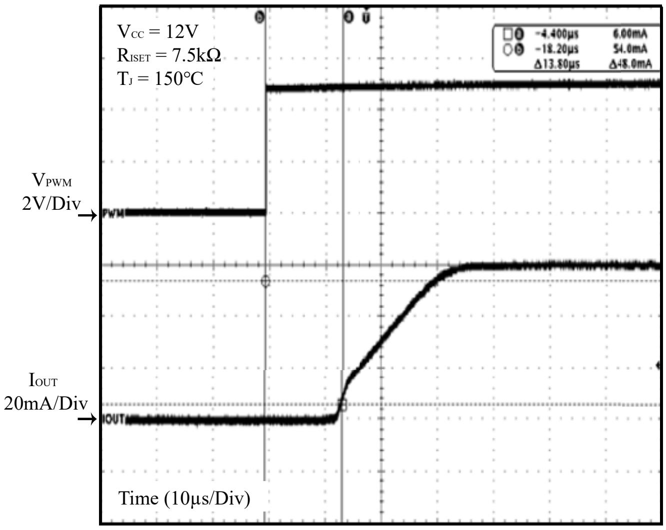


Figure 32 PWM On

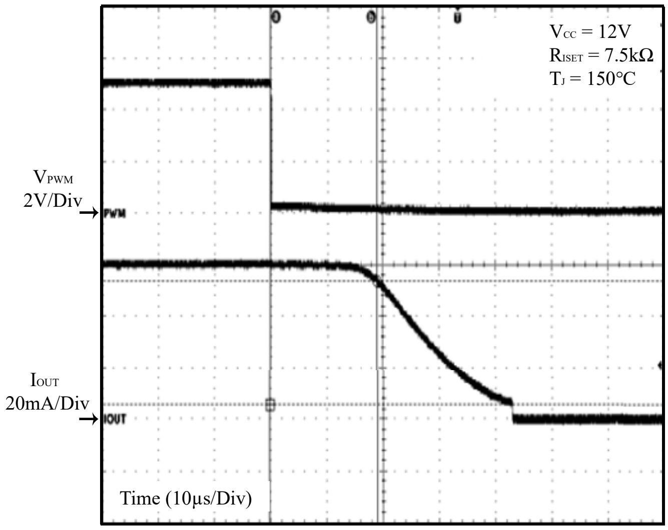


Figure 33 PWM Off

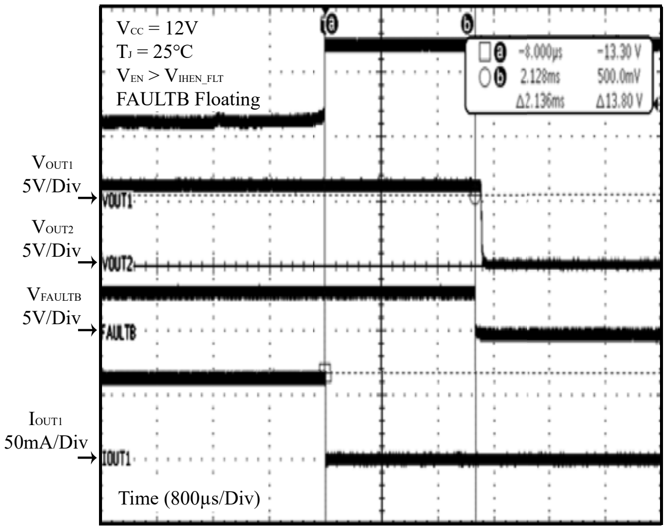


Figure 34 Output Open

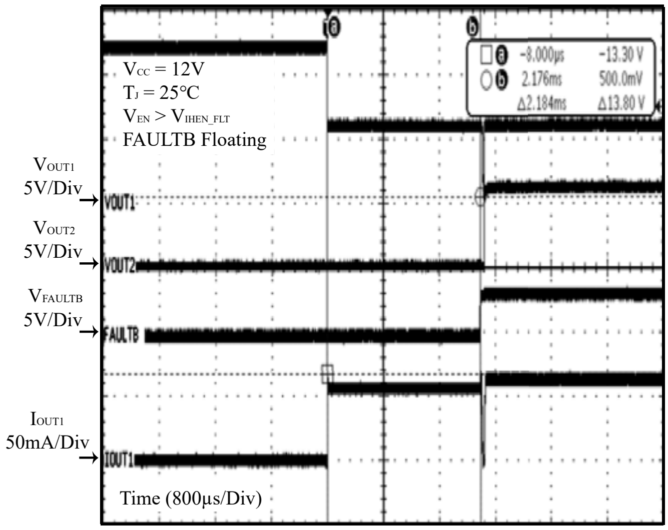


Figure 35 Output Open Remove

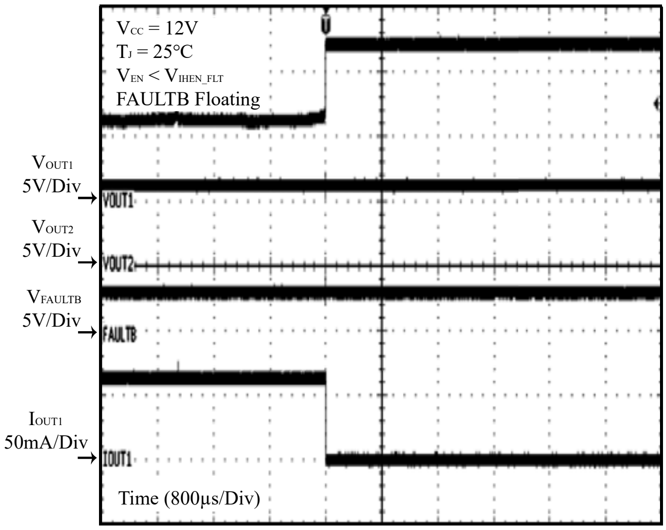


Figure 36 Output Open

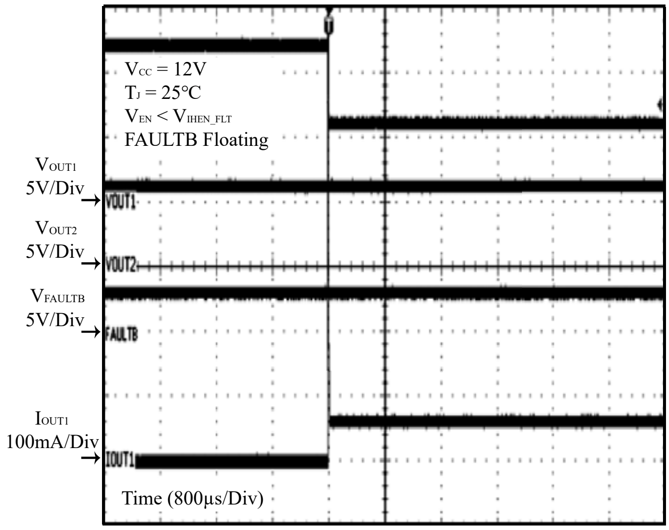


Figure 37 Output Open Remove

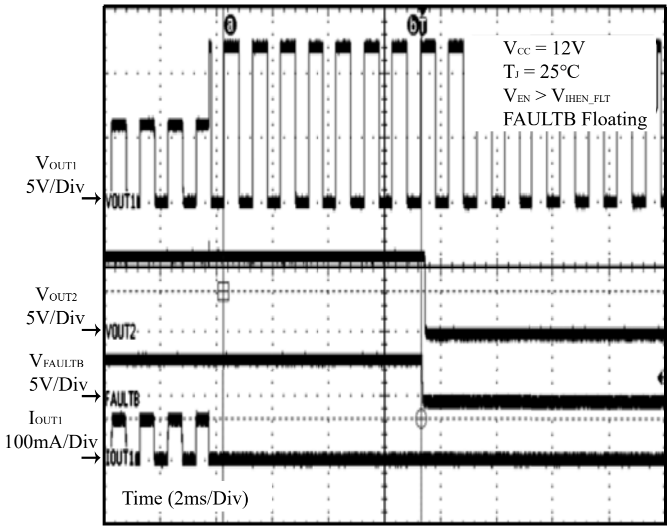


Figure 38 Output Open (PWM Dimming)

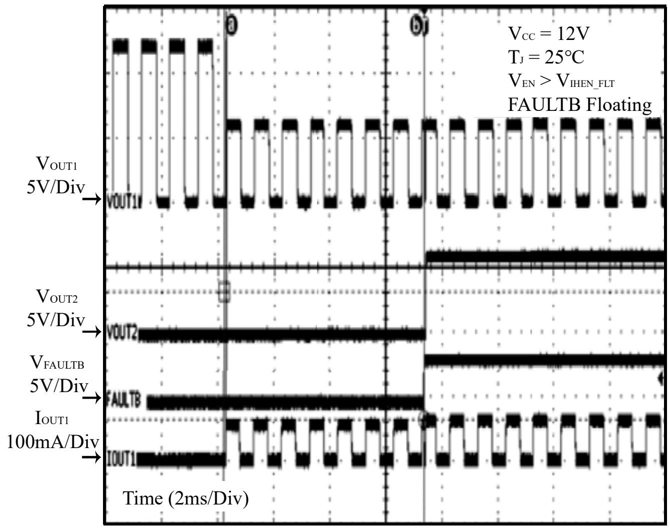


Figure 39 Output Open Remove (PWM Dimming)

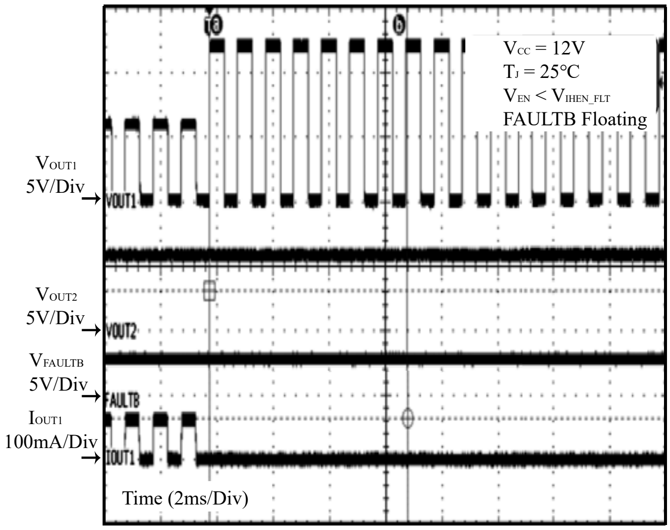


Figure 40 Output Open (PWM Dimming)

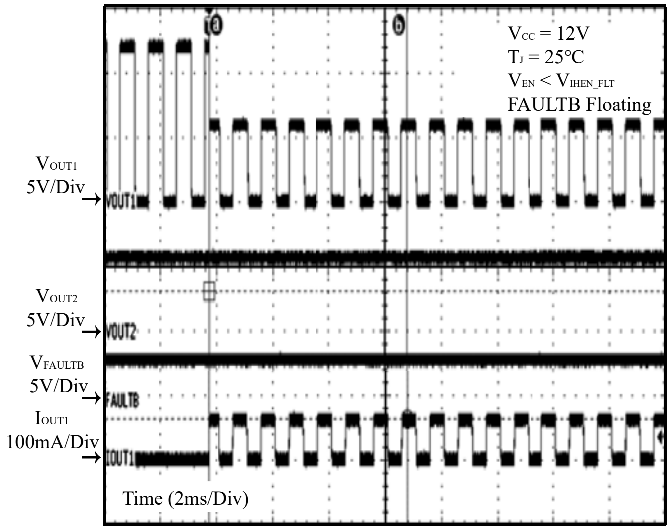


Figure 41 Output Open Remove (PWM Dimming)

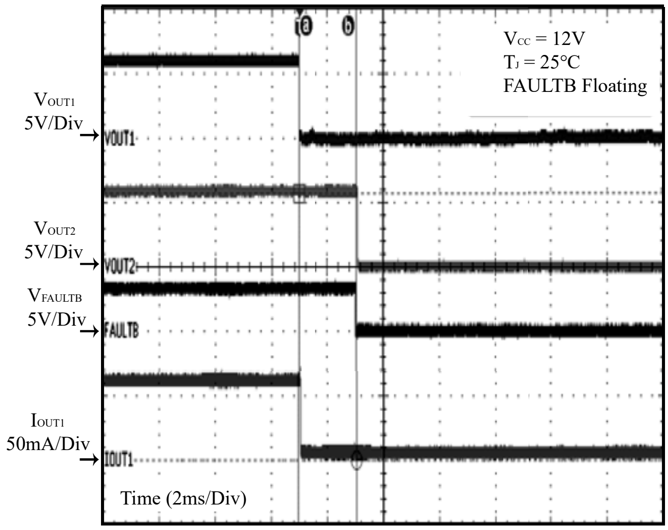


Figure 42 LED Short

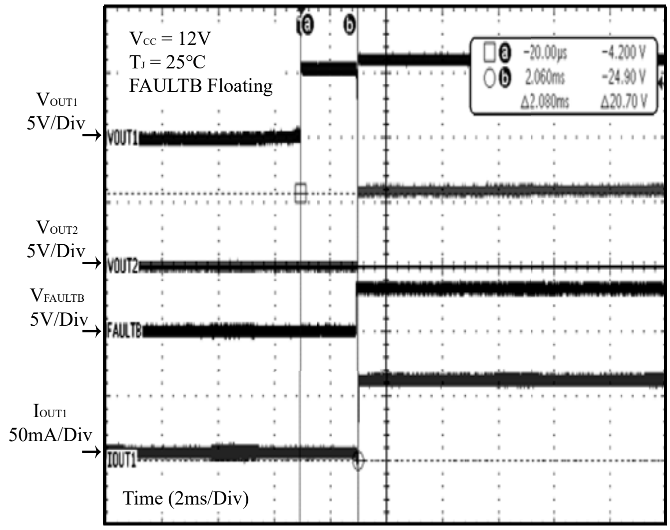


Figure 43 LED Short Remove

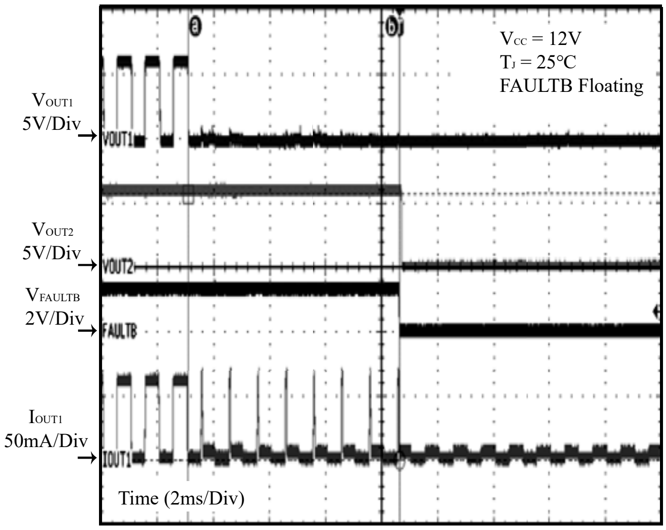


Figure 44 LED Short (PWM Dimming)

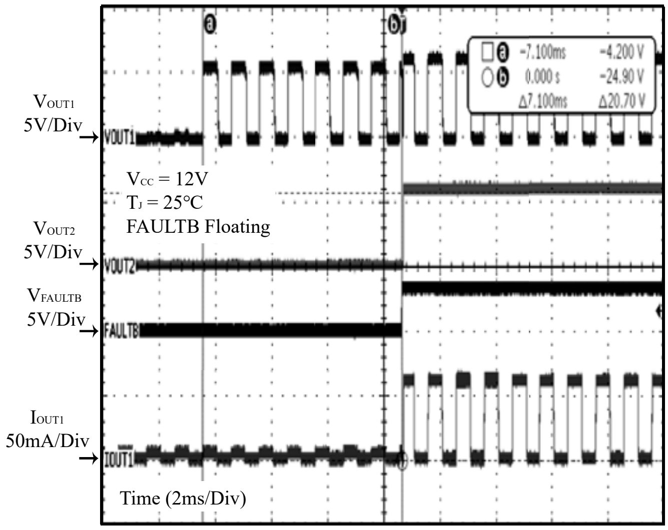


Figure 45 LED Short Remove (PWM Dimming)

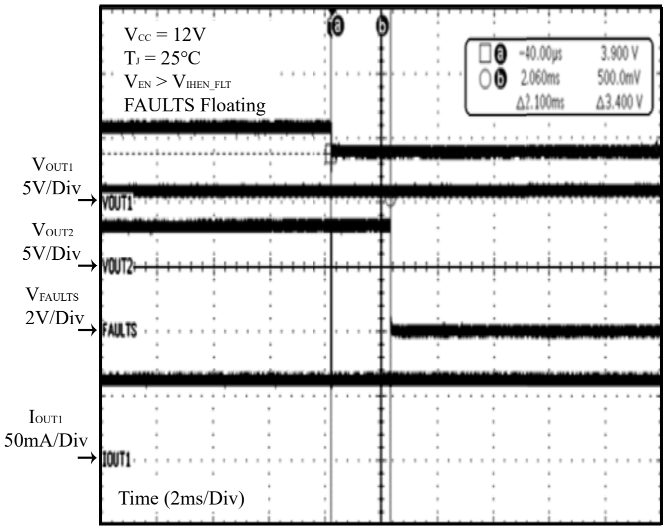


Figure 46 Single LED Short

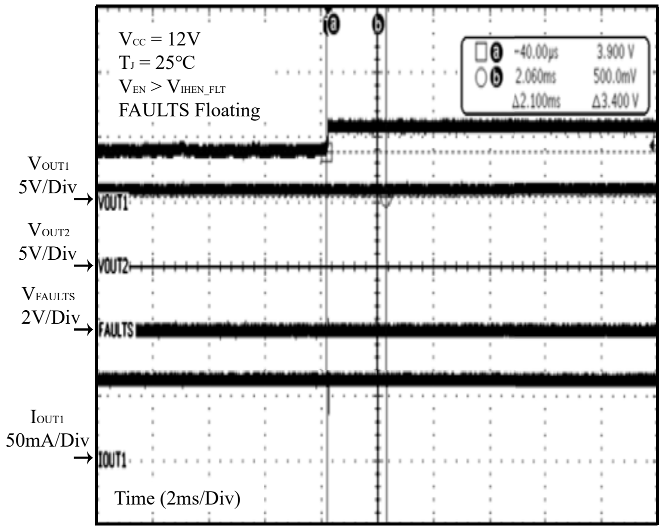


Figure 47 Single LED Short Remove

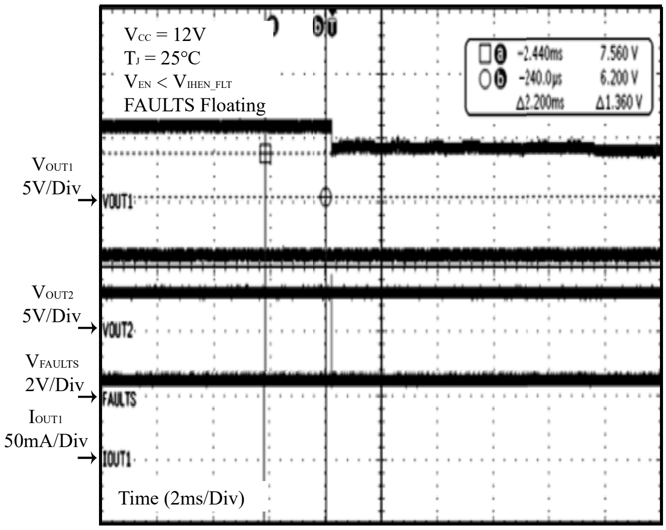


Figure 48 Single LED Short

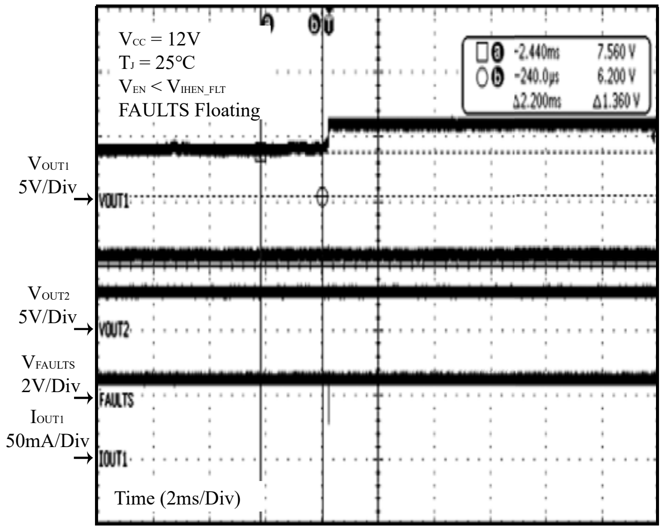


Figure 49 Single LED Short Remove

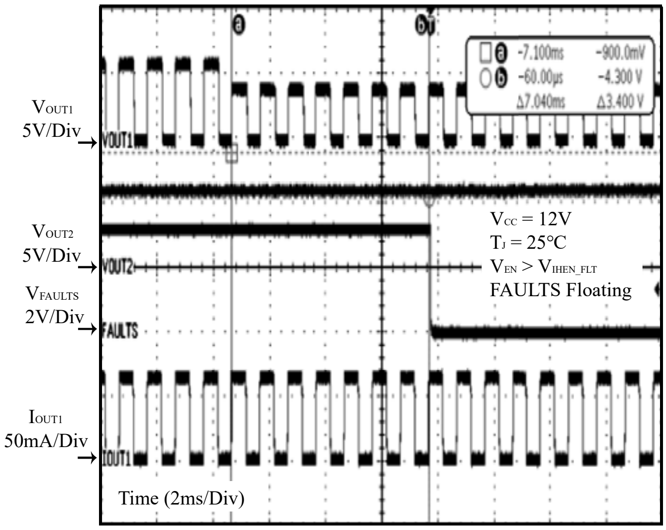


Figure 50 Single LED Short (PWM Dimming)

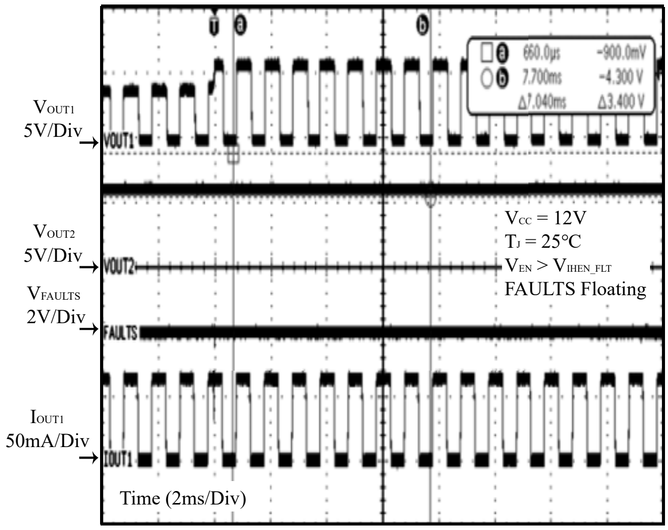


Figure 51 Single LED Short Remove (PWM Dimming)

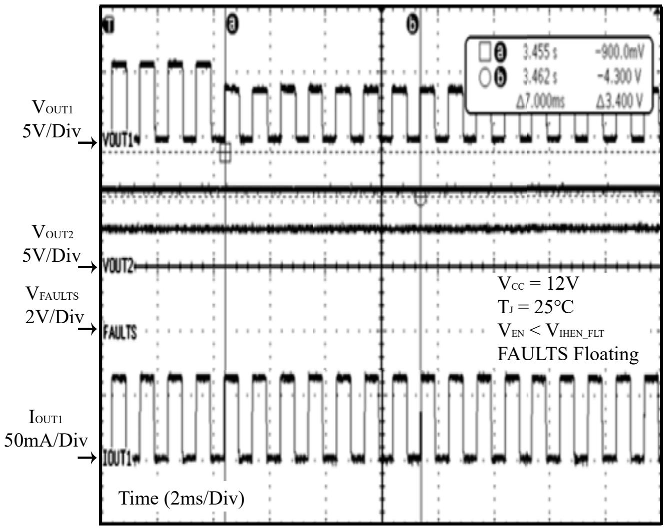


Figure 52 Single LED Short (PWM Dimming)

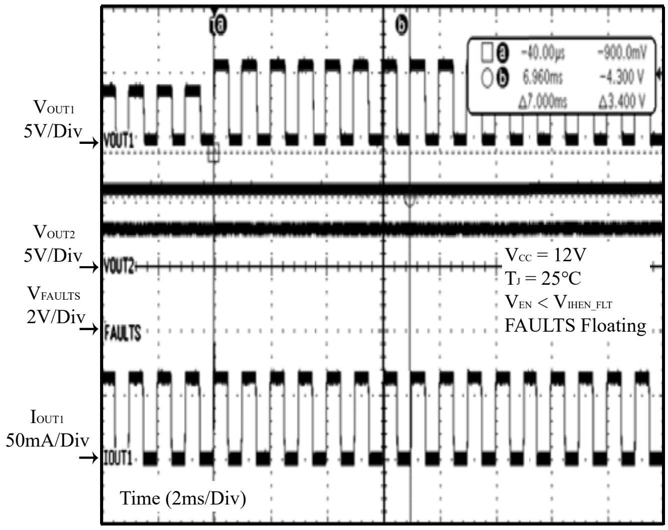


Figure 53 Single LED Short Remove (PWM Dimming)

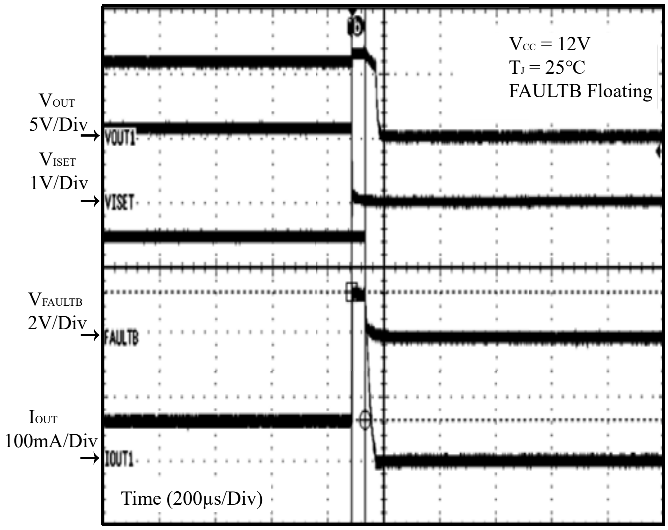


Figure 54 RISET Short

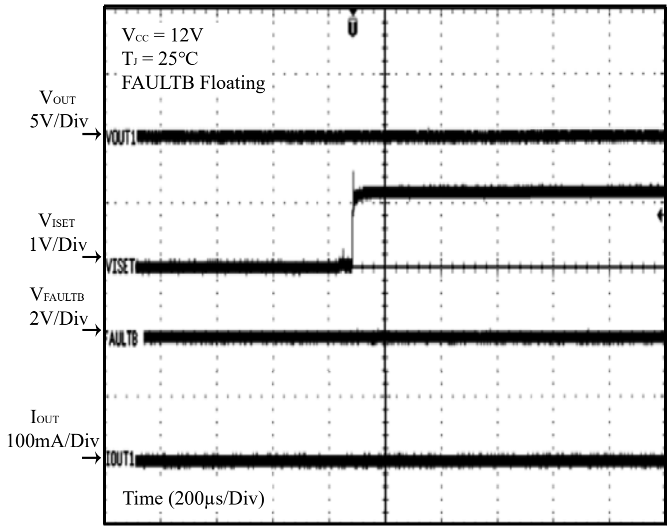


Figure 55 RISET Short Remove

APPLICATION INFORMATION

The IS32LT3144 is a three-channel constant current LED driver with individual PWM dimming, designed for a single string or multiple strings of high brightness LEDs in automotive lighting applications. A single resistor R_{ISET} is able to simultaneously set the output current of all output channels, up to 150mA per channel. A high-side current source output architecture allows common-cathode LED string connection to ground. So, the application only requires a single return wire instead of one return wire per LED string that a driver with low-side current sink output architecture would need. The advanced control loop allows high accuracy between channels and devices. A separate PWM pin can be used to dim or enable/disable each channel. A proper DC voltage on the analog dimming pin, ICTRL, can simultaneously configure the output current of all channels. The IS32LT3144 monitors various fault conditions and reports on the FAULTB and FAULTS pins.

OUTPUT CURRENT SETTING

The regulated maximum output current (up to 150mA) from each output channel is simultaneously set by the current setting resistor R_{ISET}. The R_{ISET} resistor value can be calculated using the following equation:

$$R_{ISET} = \frac{V_{ISET\_REF}}{I_{OUT}+0.22} \times 415 - 0.13 \qquad (1)$$

(3.04kΩ ≤ R_{ISET} ≤ 46.56kΩ)

Where I_{OUT} is the desired output current of each output channel in mA and R_{ISET} is in kΩ. V_{ISET_REF} is the ISET pin reference voltage, 1.15V typical.

It is recommended that R_{ISET} be a 1% accuracy resistor with good temperature characteristic to ensure stable and precise output current. On the PCB layout, this R_{ISET} resistor must be placed as close to ISET pin and GND pin as possible to avoid noise interference and ground bounce.

The device is protected from an output overcurrent condition caused by R_{ISET} resistor. The output current is limited to an I_{OUT_L} value of 240mA (Typ.) for cases when a low value resistor is connected to ISET and GND pins or ISET pin is shorted to ground.

EN PIN

The EN pin is an enable input for the device, pull it lower than V_{ILEN} to force the device into shutdown mode with an ultralow shutdown current; pull it higher than V_{IHEN} to enable the device, but the fault detection of the LED string open and single LED short is not enabled until increasing the EN pin voltage to higher than V_{IHEN_FLT}. When the EN pin is brought below V_{ILEN_FLT}, the fault detection of the LED string open and single LED short is disabled. Therefore, a proper resistor divider (R_{UV1} and R_{UV2}) connected from VCC pin to EN pin can set a fault UVLO function for LED string open and single LED short fault protection, which can prevent insufficient V_{CC} falsely triggering LED string open and single LED short detection. The fault UVLO voltage threshold is programmed by the resistor divider.

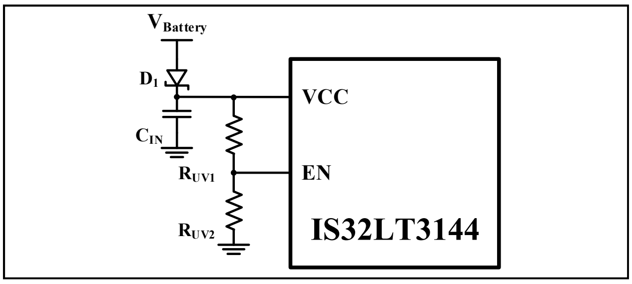


Figure 56 Fault UVLO Setting

$$V_{UVLO\_FLTF} = V_{ILEN\_FLT} \times \frac{R_{UV1}+R_{UV2}}{R_{UV2}} \qquad (2)$$

$$V_{UVLO\_FLTR} = V_{IHEN\_FLT} \times \frac{R_{UV1}+R_{UV2}}{R_{UV2}} \qquad (3)$$

It is recommended to set V_{UVLO_FLTF} at least 0.5V higher than the LED string voltage. Choose R_{UV1} and R_{UV2} to be 1% accuracy resistors with good temperature characteristic to ensure a stable and precise detection. On the PCB layout, this resistor divider must be placed as close to EN pin as possible to avoid noise interference.

The EN pin is high-voltage tolerant. If the shutdown mode and fault UVLO function are unused, directly connect the EN pin to the VCC pin. However, due to the inherent parasitic ESD diode across the EN pin and VCC pin, if a voltage applied on EN pin is possibly higher than the VCC pin voltage at any time, a series resistor (recommended value is 10kΩ) is required to limit the current flowing into it. This series resistor is recommended to be added in most applications.

PWM DIMMING

The device features a separate PWM dimming control pin for each output channel. PWM pin control the corresponding output channel. The PWM pin voltage should be higher than V_{IHPWM} to enable the corresponding output channel and lower than V_{ILPWM} to disable it. If any output channel is unused, tie the corresponding PWM pin to ground to disable it and connect the OUTx pin to the corresponding SENSx pin.

An external PWM signal on the PWMx pins can be used to modulate the output current to dim the LED light output. The PWM dimming LED current is based on the PWM signal's duty cycle and can be calculated by the following Equation:

$$I_{OUT\_PWM} = I_{OUT} \times D_{PWM} \qquad (4)$$

Where D_{PWM} is the duty cycle of PWM signal.

The recommended frequency range of the external PWM signal is 100Hz~1kHz and the duty cycle can be from 0 to 100%. Due to the output's current slew rate control for EMI consideration plus the propagation delay time from PWM rising edge to the output activity, a lower frequency PWM will provide a better dimming linearity and contrast ratio.

All PWMx pins are high-voltage tolerant. If the PWM dimming of any channel is not implemented, directly connect its corresponding PWM pin to the VCC pin. However, due to the inherent parasitic ESD diode across PWMx pin and VCC pin, if a voltage applied on PWMx is possibly higher than the VCC pin voltage at any time, a series resistor (recommended value is 10kΩ) is required for each pin to limit the current flowing into it. This series resistor is recommended to be added in most applications.

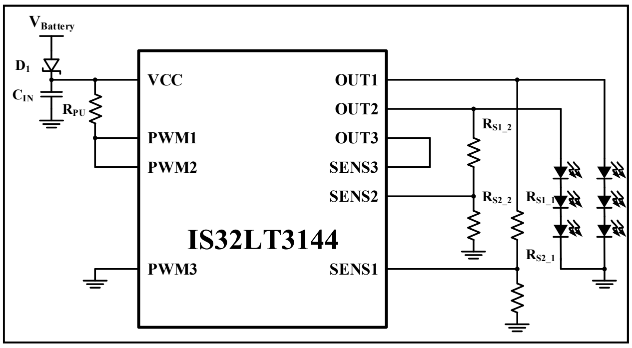


Figure 57 Example of No PWM Dimming and OUT3 Unused

VCC UNDERVOLTAGE LOCKOUT

The IS32LT3144 features an undervoltage lockout (UVLO) function on the VCC pin to prevent indeterminate operation at low input voltages. The UVLO threshold is an internally fixed value and cannot be adjusted. The device is enabled when the V_{CC} voltage exceeds (V_{UVLO}+V_{UVLO_HY}) (Typ. 4.3V) and disabled when the V_{CC} voltage falls below V_{UVLO} (Typ. 4.1V).

Besides this internal, fixed UVLO, it may be desirable to externally set a higher UVLO threshold for some applications. The PWMx pins have precise threshold, which can be used to define an external undervoltage-lockout (UVLO) function for its corresponding output channel with a resistor voltage divider between VCC and GND with the center connected to the PWMx pin. As shown in Figure 58.

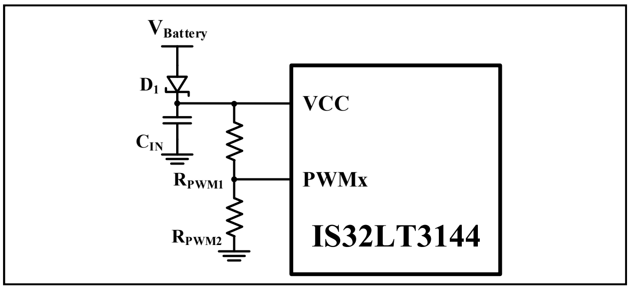


Figure 58 External UVLO Defined by PWMx Pins

The external UVLO threshold voltage can be computed by the following equations:

$$V_{UVLO\_EXF} = V_{ILPWM} \times \frac{R_{PWM1}+R_{PWM2}}{R_{UV2}} \quad (5)$$

$$V_{UVLO\_EXR} = V_{IHPWM} \times \frac{R_{PWM1}+R_{PWM2}}{R_{PWM2}} \quad (6)$$

The corresponding output channel is enabled when the V_{CC} voltage exceeds V_{UVLO_EXR}, and disabled when the V_{CC} voltage falls below V_{UVLO_EXF}.

It is recommended that R_{PWM1} and R_{PWM2} be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. On the PCB layout, this resistor divider must be placed as close as possible to the corresponding PWM pin to avoid noise coupling into the UVLO detection.

ANALOG DIMMING

The IS32LT3144 also offers an analog dimming function on input pin, ICTRL, whose dimming voltage range is 0.6V to 1.9V. The output current of all channels can be simultaneously regulated by the ICTRL pin voltage. If the ICTRL pin is pulled up above 1.9V, analog dimming is disabled and the output current is given by Equation (1). When the ICTRL pin voltage is driven below 1.9V, V_{ICTRL} will proportionally regulate the output current as given by the following Equation:

$$I_{OUT\_ICTRL} = I_{OUT} \times \frac{V_{ICTRL}-0.44V}{1.46V} \quad (7)$$

Note that the relative current accuracy decreases with the decreasing current sense voltage threshold due to the offset of the internal circuit. Therefore, the recommended minimum analog dimming level is around 30%.

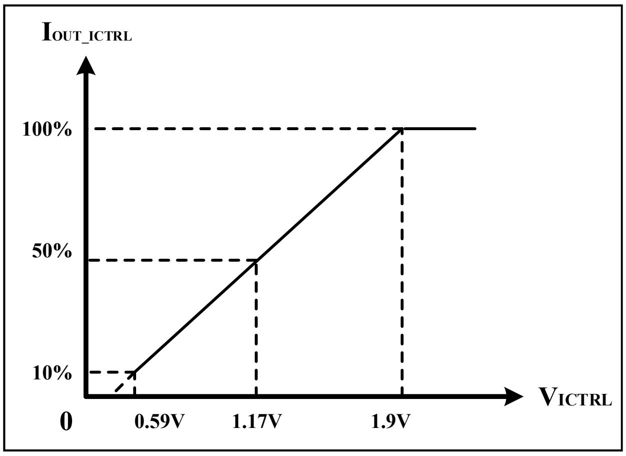


Figure 59 Analog Dimming Graph

Never leave the ICTRL pin floating. The ICTRL pin is high-voltage tolerant. If the analog dimming function is not implemented, connect the ICTRL pin to the VCC pin. However, due to the inherent parasitic ESD diode across ICTRL pin and VCC pin, if a voltage applied on ICTRL pin is possibly higher than the VCC pin voltage at any time, a series resistor (recommended value is 10kΩ) is required to limit the current flowing into it. This series resistor is recommended to be added in most applications.

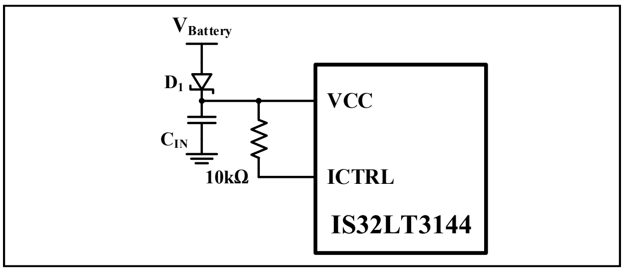


Figure 60 ICTRL Pin Unused

It is recommended to add a 10nF ceramic capacitor from the ICTRL pin to GND to bypass any high frequency noise, especially if the analog voltage level comes from a long copper trace. This 10nF capacitor should be placed as close to the ICTRL pin as possible. The following are some application scenarios for use of the analog dimming function.

LED Binning:

The ICTRL pin can be used to fine tune the output current during mass-production. LEDs are typically sorted into various bins of different luminous intensity and forward voltage. To correct the brightness deviation during mass-production, the mean output current can be adjusted by adjusting the voltage level on the ICTRL pin. As shown in Figure 61, fix the R_{ICTRL1} value and solder different value R_{BIN} resistor to adjust and maintain the same lumen output across different LED bins. This R_{BIN} resistor can be placed on the LED board.

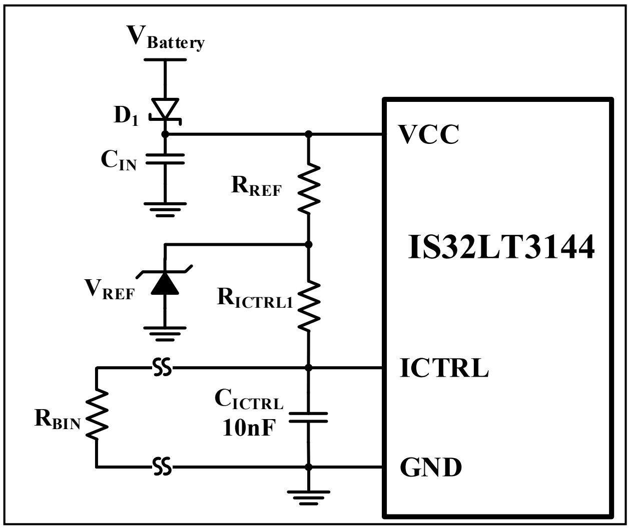


Figure 61 Analog Dimming For LED Binning

Over Temperature Thermal Roll-Off:

The ICTRL pin can also be used in conjunction with a NTC thermistor to provide over temperature current roll-off protection for the LED load or the system. As Figure 62.

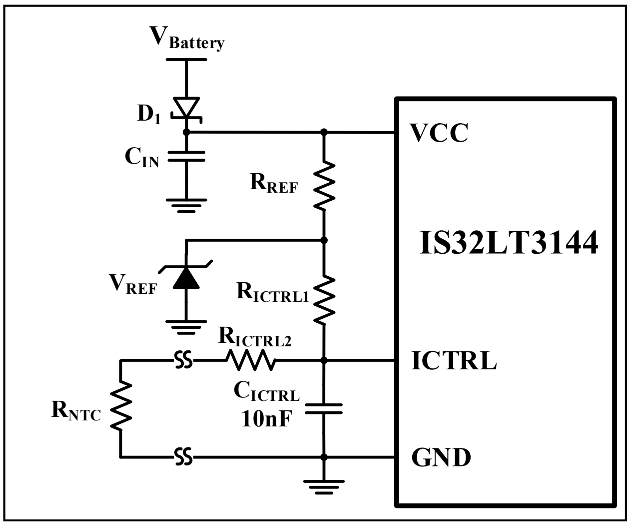


Figure 62 ICTRL Pin with NTC for Thermal Roll-Off Protection

For example, assume the desired current roll-off temperature threshold is T_R and the NTC thermistor resistance is R_{NTCR} at this temperature (R_{NTCR} can be found in the NTC thermistor datasheet), then R_{ICTRL1} and R_{ICTRL2} can be calculated by:

$$R_{ICTRL1} = \frac{(R_{NTCR}+R_{ICTRL2})\times(V_{REF}-1.9V)}{1.9V} \quad (8)$$

For a given NTC thermistor, the R_{ICTRL1} resistor will adjust the current roll-off temperature threshold. The larger R_{ICTRL1} the lower the current roll-off temperature threshold. The R_{ICTRL2} resistor is optional to be used to adjust current derating slope. The larger R_{ICTRL2} the flatter the current derating slope. If R_{ICTRL2} is not used, tie the NTC thermistor directly to ICTRL pin.

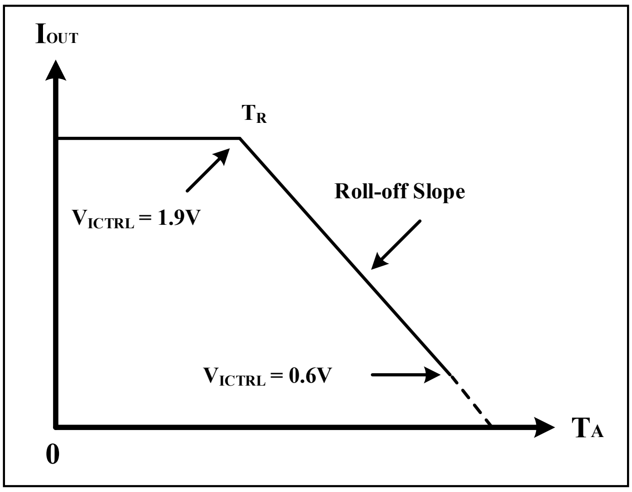


Figure 63 NTC Thermal Roll-Off Protection

The NTC thermistor should be placed next to the component to be monitored. Such as the LED board, driver board and so on.

Dual Brightness Level Output:

In automotive applications, some lamps require a dual brightness output. For instance, the daytime running light (DRL) and the position light (POL) can both use the same LED string, since these two lamps won't be active at the same time. The DRL is active in the daytime, while POL is active with lower brightness in the nighttime. Two brightness levels are selected by two independent power supply rails. The analog dimming can be used for this dual brightness output function.

As Figure 64, when the input logic to the GATE of the MOSFET Q_1 is high, R_{ICTRL3} resistor is shorted by Q_1. The output current is determined by the resistor divider R_{ICTRL1} and R_{ICTRL2}. If the GATE of the switch Q_1 is pulled low, the output current is determined by the resistor divider R_{ICTRL1}, R_{ICTRL2} and R_{ICTRL3} the result is a higher brightness.

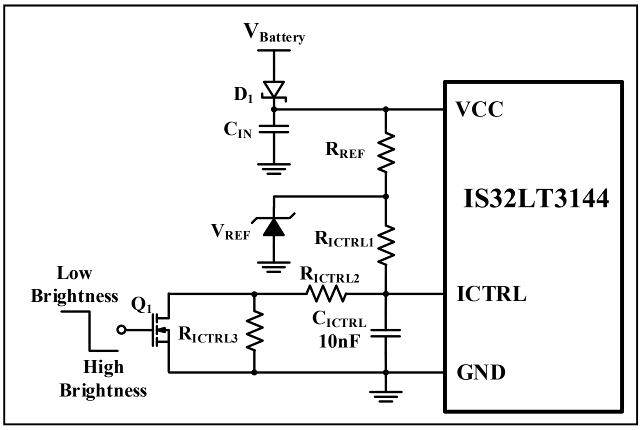


Figure 64 ICTRL Pin for Dual Brightness Output

To implement analog dimming by the ICTRL pin, it needs a precise reference voltage source, V_{REF}, which can be derived from the VCC by a TL431 device. The recommended V_{REF} value is 4V~5V.

FAULT PROTECTION AND REPORTING

For robust system reliability, the IS32LT3144 integrates the detection circuitry to protect various fault conditions and report the fault conditions on the fault reporting pins, FAULTB and FAULTS, which can be monitored by an external host. The fault reporting pins will go low when the device detects a fault condition. FAULTS is a dedicated fault reporting pin for single LED short fault condition and the FAULTB is for general fault conditions, including LED string open/short, current setting resistor short and thermal shutdown. Both fault reporting pins have an internal weak current source I_{PU} pulled up to an internal voltage source V_{FLT_PU} (Typical 3.3V) and an internal strong current sink I_{PD} pulled down to ground. As shown in Figure 65.

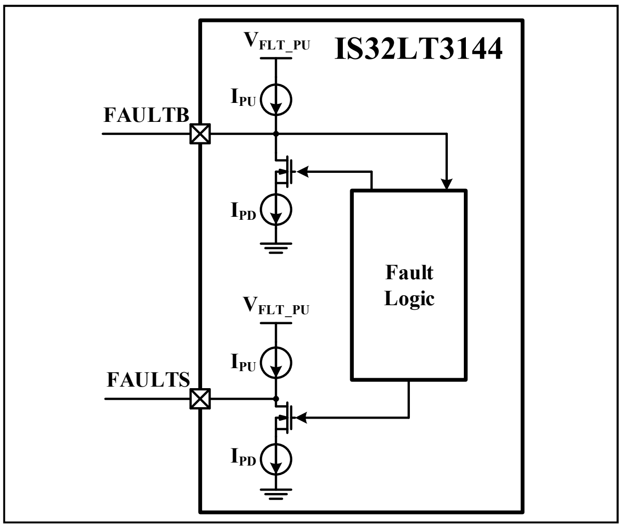


Figure 65 FAULTB and FAULTS Pin Internal Circuit

The FAULTB pin also supports and input function. As long as the FAULTB pin voltage drops below the logic input low level V_{ILFLTB}, no matter if it is pulled down by an external circuit or the internal pull-down current sink I_{PD}, all output channels (excluding the failing channel) will be turned off to satisfy the "one fail all fail" operating requirement. For lighting systems with multiple IS32LT3144 drivers which requires the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection. A fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the system "one fail all fail" operating requirement. The allowed fault reporting parallel pin (FAULTB and FAULTS) connection is up to 15 devices.

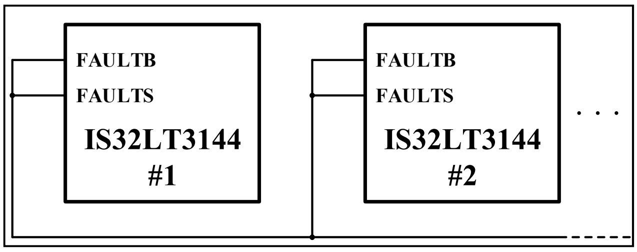


Figure 66 FAULTB/FAULTS Parallel Connection

If the FAULTB pin is externally forced high (for example, pulled up by a 1kΩ resistor to VCC) so that the internal pull-down current sink I_{PD} of fault actions is not capable to pull the FAULTB pin below the logic input low level V_{ILFLTB}, the fault actions (including LED string open/short fault) will keep other channels normal operation that satisfies the "one fail other on" operating requirement. Refer to Table 1 for detailed fault actions.

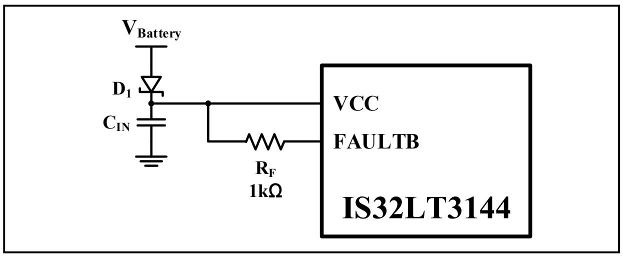


Figure 67 Externally Forced FAULTB High

LED STRING OPEN PROTECTION

The LED string open detection is enabled if the VCC pin voltage is greater than V_{UVLO_FLTR}, and disabled if the VCC voltage drops below V_{UVLO_FLTF}.

In case of any LED string is open, the corresponding OUTx pin will be pulled up close to VCC pin voltage by the current source. When V_{CC}> V_{UVLO_FLTR} and the VCC pin to OUTx pin voltage drop, (V_{CC}-V_{OUTx}), falls below the LED string open detection voltage, V_{OCD}, and persists for longer than the deglitch time t_{OCD} (2ms when PWM is 100% on or one PWM on-time is more than 2ms, or seven continuous PWM duty cycles when in PWM dimming mode), the FAULTB pin will go low to report the fault condition. The open channel will stay on and the other channels will be turned off due to the FAULTB pin low, that satisfies "one fail all fail" condition. If the FAULTB pin is externally forced high, the other channels will remain turned on that satisfies the "one fail other on" condition.

The device will recover to normal operation and FAULTB pin will go back high once the open condition is removed, (V_{CC}-V_{OUTx}) rising above the LED string open detection voltage, (V_{OCD}+V_{OCD_HYS}).

Note that the device can detect a LED string open if the string forward voltage of the LED string is close to or greater than the VCC voltage. When the input voltage V_{CC} is lower than V_{UVLO_FLTF}, the device shields LED string open fault detection. Even though a LED string open fault occurs, the device does not report the fault with the FAULTB pin.

LED STRING SHORT PROTECTION

The LED string short condition is detected if any one of the OUTx pin voltage is lower than LED string short detection voltage, V_{SCD}. Once a short condition occurs and persists for longer than the deglitch time t_{SCD} (2ms when PWM is 100% on or one PWM on-time is more than 2ms, or seven continuous PWM duty cycles when in PWM dimming mode), the FAULTB pin will go low to report the fault condition and the faulty channel will reserve a small current I_{RTR} for recovery detection. The other channels will be turn off due to the FAULTB pin low, that satisfies "one fail all fail". If the FAULTB pin is externally forced high, the other channels will remain turned on that satisfies the "one fail other on" condition.

The device will recover to normal operation and FAULTB pin will go back to high once the short condition is removed, the OUTx pin voltage rising above the LED string short detection voltage, (V_{SCD}+V_{SCD_HYS}).

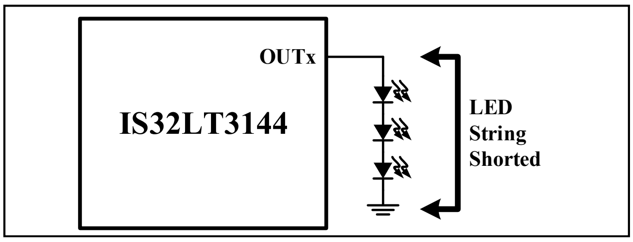


Figure 68 LED String Shorted

SINGLE LED SHORT PROTECTION

The IS32LT3144 supports independent single LED short detection for each channel, which is enabled if the VCC pin voltage is greater than V_{UVLO_FLTR} and disabled if the VCC voltage drops below V_{UVLO_FLTF}. There are three comparators (CMPx) inside the device used to monitor each LED string voltage with external resistor dividers connected to the SENSx pins.

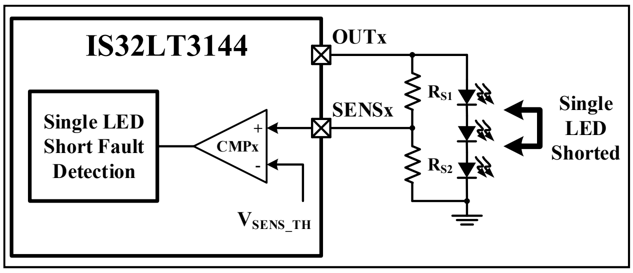


Figure 69 Single LED Short Detection Circuit

In case of V_{CC}> V_{UVLO_FLTR} and any one of SENSx pins voltage drops below the internal reference V_{SENS_TH} persists for longer than the deglitch time t_{SENS} (2ms when PWM is 100% on or one PWM on-time is more than 2ms, or seven continuous PWM duty cycles when in PWM dimming mode), the FAULTS pin will be latched in low state to report the fault condition but no other action results. The FAULTS pin latched low is not self-clearing, a toggling of EN or power cycle is required to clear FAULTS.

If the FAULTS pin is externally tied to the FAULTB pin, the FAULTS pin will pull the FAULTB pin low to turn off all output channels (including the faulty channel) to satisfy the "one fail all fail" operating requirement.

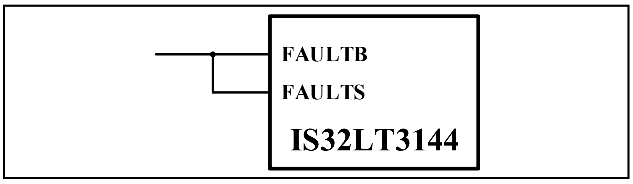


Figure 70 FAULTS Tied to FAULTB for "One fail all Fail"

To achieve proper single LED short detection and avoid false triggering, the resistor divider, R_{S1} and R_{S2}, should be chosen according to the minimum and maximum of the LED forward voltage:

$$(N-1) \times V_{F\_MAX} < V_{SENS\_TH} \times \frac{R_{S1}+R_{S2}}{R_{S2}} < N \times V_{F\_MIN} \quad (9)$$

Where, N is the number of LEDs in the string. V_{F_MAX} and V_{F_MIN} are the maximum and minimum forward voltage of a single LED.

It is recommended that R_{S1} and R_{S2} be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. On the PCB layout, this resistor divider must be placed as close as possible to the corresponding SENSx pin to avoid noise coupling into the single LED short detection.

When multiple output channels are combined to provide a higher current to one LED string, the SENSx pins can share one resistor divider for single LED short fault detection.

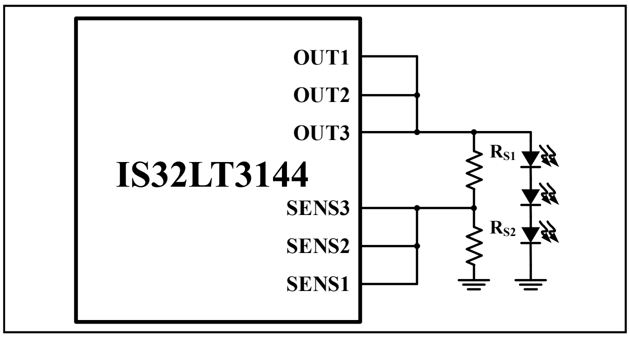


Figure 71 Single LED Short Detection Circuit of Multiple Channels in Parallel

When the input voltage V_{CC} is lower than V_{UVLO_FLTF}, the device shields single LED short fault detection. Even though a single LED short fault occurs, the device does not report the fault with the FAULTS pin.

All SENSx pins are high-voltage tolerant. If the single LED short protection of any channel is unused, the SENSx pin should be directly connected to its corresponding OUTx pin. Figure 72 shows connection when the single LED short protection of the OUT3 is unused.

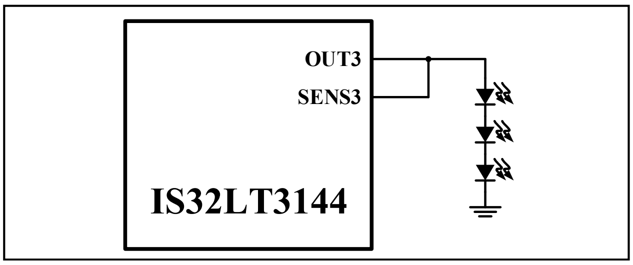


Figure 72 SENS3 Pin Unused Example

ISET PIN SHORT PROTECTION

The device is protected from an output overcurrent condition caused by R_{ISET} resistor. Each output channel current is limited to an I_{OUT_L} value of 240mA in case of the ISET pin is shorted or too low value resistor (<R_{ISET_SC}) is connected to the ISET pin. If the condition persists for longer than fault detection deglitch time (typ. 40µs), the ISET pin short protection will be triggered. All output channels will be latched in off state and the FAULTB pin will go low to report the fault condition.

Both ISET pin short fault protection and reporting are not self-clearing a toggling of EN or power cycle is required.

VCC OVERVOLTAGE CURRENT DERATING PROTECTION

In automotive applications, the nominal battery voltage range is about 9V to 16V. However, electrical and radio-frequency disturbance frequently occur in vehicle environment that results in the supply voltage jumping over 16V. Such as load dump case, it could raise up the supply voltage over 40V. High input voltage results in large power dissipation on the device. The IS32LT3144 integrates a VCC overvoltage current derating protection to avoid thermal runaway on the device.

In case the VCC voltage exceeds the internal overvoltage threshold, the device will start to gradually reduce the output current down by 50%×I_{OUT} (Typ.), following the increasing V_{CC}. As shown in Figure 73.

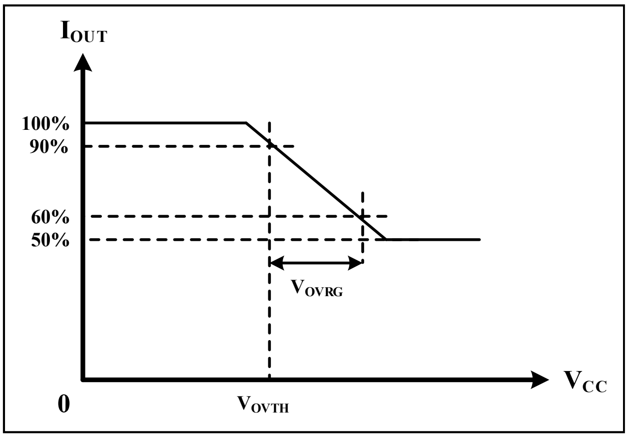


Figure 73 V_{CC} Overvoltage Protection

VCC overvoltage current derating protection won't be reported via fault reporting pins.

THERMAL SHUTDOWN

In the event that the junction temperature exceeds T_{SD} (Typ. 175˚C), all output channels will go to the OFF state and FAULTB pin will pull low to report the fault condition. At this point, the IC presumably begins to cool off. Any attempt to toggle the channels back to the source condition before the IC has cooled to below (T_{SD}-T_{SD_HYS}) (Typ. 160˚C) will be blocked and the IC will not be allowed to restart. The FAULTB pin will recover high once the IC has cooled down.

THERMAL ROLL-OFF PROTECTION

The device integrates thermal shutdown protection to prevent the device from overheating. In addition, to preventing the LEDs from flickering due to rapid thermal changes, the device also includes a programmable thermal roll-off feature to reduce power dissipation at high junction temperature.

The output current will be equal to the set value I_{OUT} as long as the junction temperature of the IC remains below the programmed thermal roll-off activation temperature threshold. If the junction temperature exceeds the threshold, the output current of all channels will begin to reduce at a rate of about typical 3.5% of I_{OUT} per °C until 20% (Typ.) of I_{OUT} following the junction temperature ramping up. Thermal roll-off protection is not reported by the fault reporting pins.

By mounting the IS32LT3144 device on the same thermal substrate as the LEDs, use of this feature can also limit the dissipation of the LEDs.

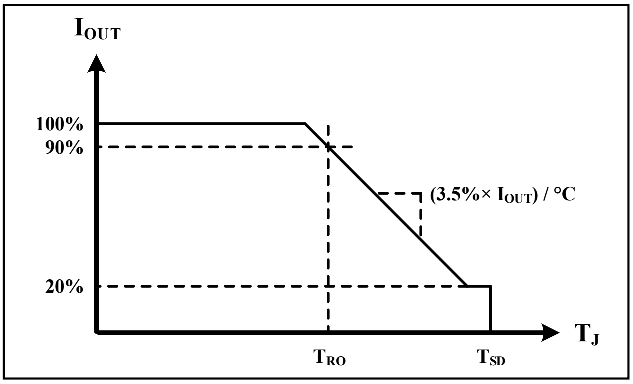


Figure 74 Junction Thermal Roll-off

Table 1 FAULT ACTION TABLE

EN Pin	Fault Type	Fault Condition	Fault Reporting Pin		Outputs State	Recovery
< V_{ILEN_FLT}	LED string open	Disabled				
< V_{ILEN_FLT}	LED string short	V_{OUTx}<V_{SCD}	FAULTB	Externally forced high	Failing string outputs I_{RTR} for recovery detection and other strings stay ON	V_{OUTx}> (V_{SCD}+V_{SCD_HY})
				Floating, goes low	Failing string outputs I_{RTR} for recovery detection and other strings turned OFF	
< V_{ILEN_FLT}	Single LED short	Disabled				
< V_{ILEN_FLT}	ISET short	ISET pin to GND resistance < R_{ISET_SC}	FAULTB	Externally forced high	All strings turned OFF	Power cycle, toggle EN pin
				Floating, latched low		
< V_{ILEN_FLT}	Thermal shutdown	T_J>T_{SD}	FAULTB	Externally forced high	All strings turned OFF	T_J< (T_{SD}-T_{SD_HYS})
				Floating, goes low		
< V_{ILEN_FLT}	Thermal roll-off	T_J>T_{RO}	-	-	Output current of all channels linearly decreases toward zero following T_J increasing	T_J<T_{RO}
< V_{ILEN_FLT}	VCC overvoltage	V_{CC}>V_{OVTH}	-	-	Output current of all channels linearly decreases toward 50% following V_{CC} increasing	V_{CC}<V_{OVTH}
>V_{IHEN_FLT}	LED string open	(V_{CC}-V_{OUTx})<V_{OCD}	FAULTB	Externally forced high	All strings stay ON	(V_{CC}-V_{OUTx}) > (V_{OCD}+V_{OCD_HY})
				Floating, goes low	Failing string stays ON and other strings turned OFF	
>V_{IHEN_FLT}	LED string short	V_{OUTx}<V_{SCD}	FAULTB	Externally forced high	Failing string outputs I_{RTR} for recovery detection and other strings stay ON	V_{OUTx}> (V_{SCD}+V_{SCD_HY})
				Floating, goes low	Failing string outputs I_{RTR} for recovery detection and other strings turned OFF	
>V_{IHEN_FLT}	Single LED short	V_{SENSx}<V_{SENS_TH}	FAULTS	Externally forced high	All strings stay ON	Power cycle, toggle EN pin
				Floating, latched low		
>V_{IHEN_FLT}	ISET short	ISET pin to GND resistance < R_{ISET_SC}	FAULTB	Externally forced high	All strings turned OFF	Power cycle, toggle EN pin
				Floating, latched low		
>V_{IHEN_FLT}	Thermal shutdown	T_J>T_{SD}	FAULTB	Externally forced high	All strings turned OFF	T_J< (T_{SD}-T_{SD_HYS})
				Floating, goes low		
>V_{IHEN_FLT}	Thermal roll-off	T_J>T_{RO}	-	-	Output current of all channels linearly decreases toward I_{RO_IMIN} following T_J increasing	T_J<T_{RO}
>V_{IHEN_FLT}	VCC overvoltage	V_{CC}>V_{OVTH}	-	-	Output current of all channels linearly decreases toward 50% following V_{CC} increasing	V_{CC}<V_{OVTH}

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3144, P_{3144}, and the package thermal resistance, θ_{JA}, as in following equations:

$$P_{3144} = V_{CC} \times I_{CC} + \sum_{x=1}^{3}(V_{CC} - V_{LEDx}) \times I_{OUT} \quad (10)$$

and,

$$T_J = T_A + \Delta T = T_A + P_{3144} \times \theta_{JA} \quad (11)$$

Where, I_{CC} is the IC quiescent current, V_{LEDx} is the voltage of the OUTx pin to ground, I_{OUT} is the output current of OUTx pin and T_A is the ambient temperature.

When operating the chip at high ambient temperatures, or when the supply voltage is high, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation at T_A=25°C can be calculated using the following equation:

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \quad (12)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{45.4°C/W} \approx 2.75W$$

for eTSSOP-16 package.

Figure 75 shows the power derating of the IS32LT3144 on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

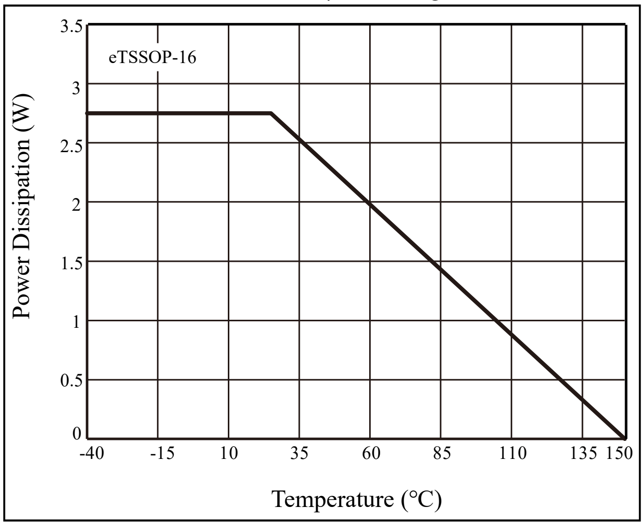


Figure 75 Dissipation Curve

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a large copper area on each side of the board directly under the IS32LT3144 and the thermal shunt resistor. Multiple thermal vias, as shown in Figure 76, will help to conduct heat from the exposed pad of the IS32LT3144 and the thermal shunt resistor to the copper on each side of the board.

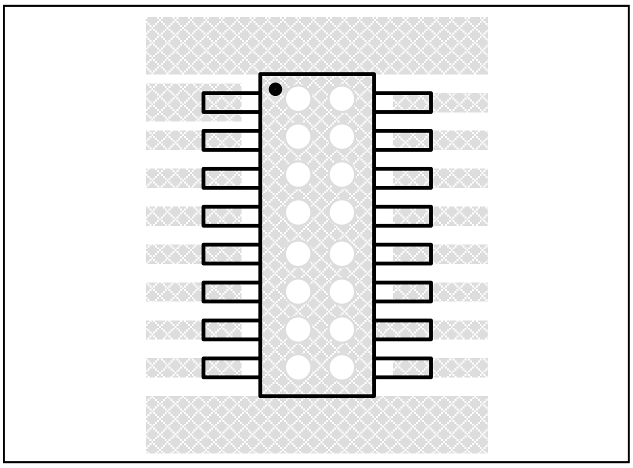


Figure 76 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

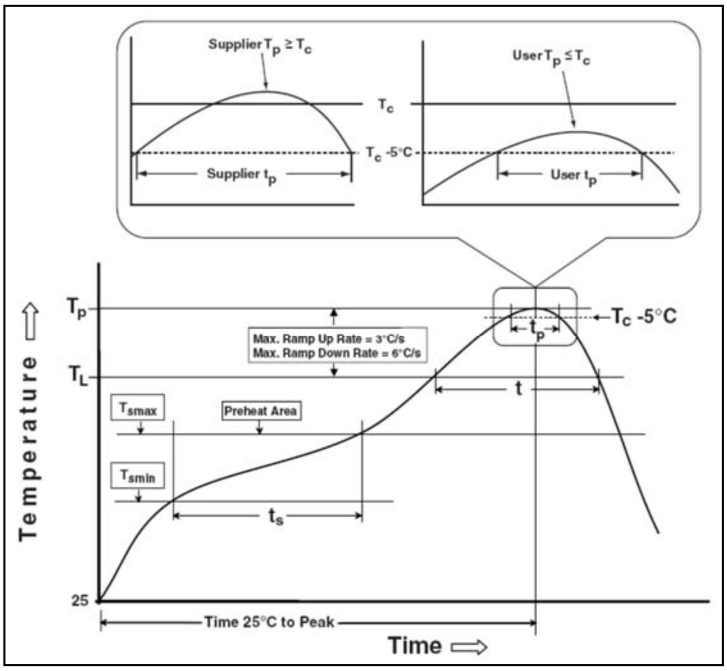
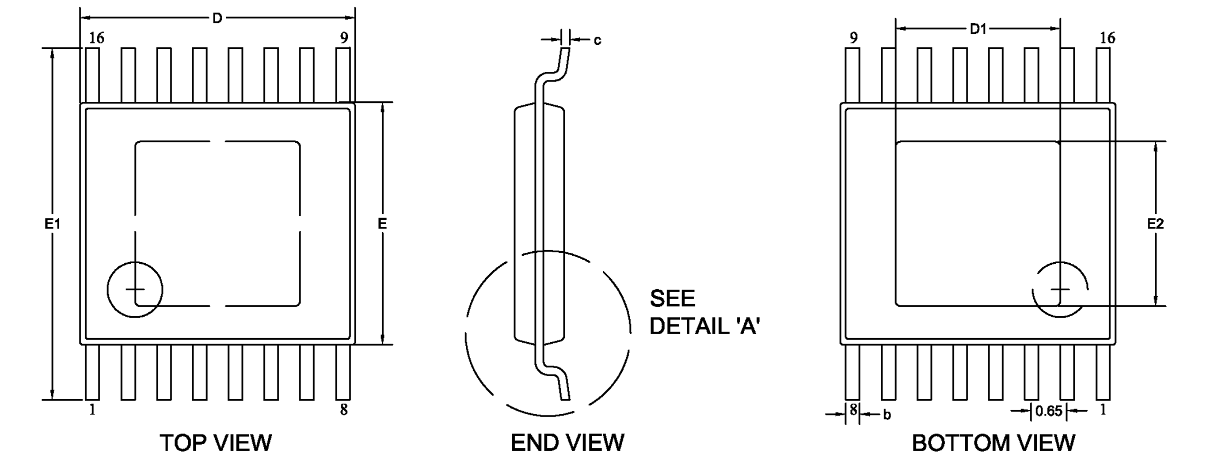


Figure 77 Classification Profile

PACKAGE INFORMATION

eTSSOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

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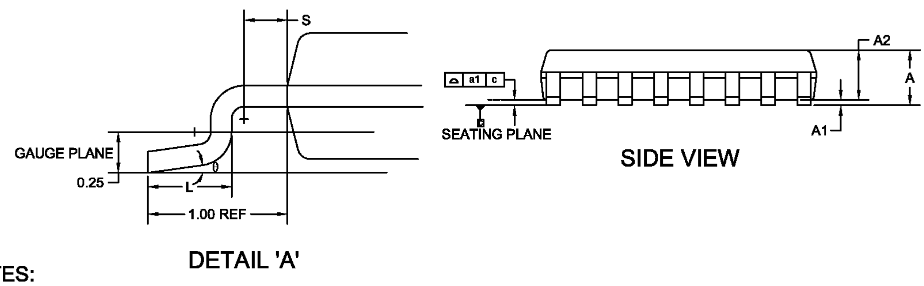


NOTES:

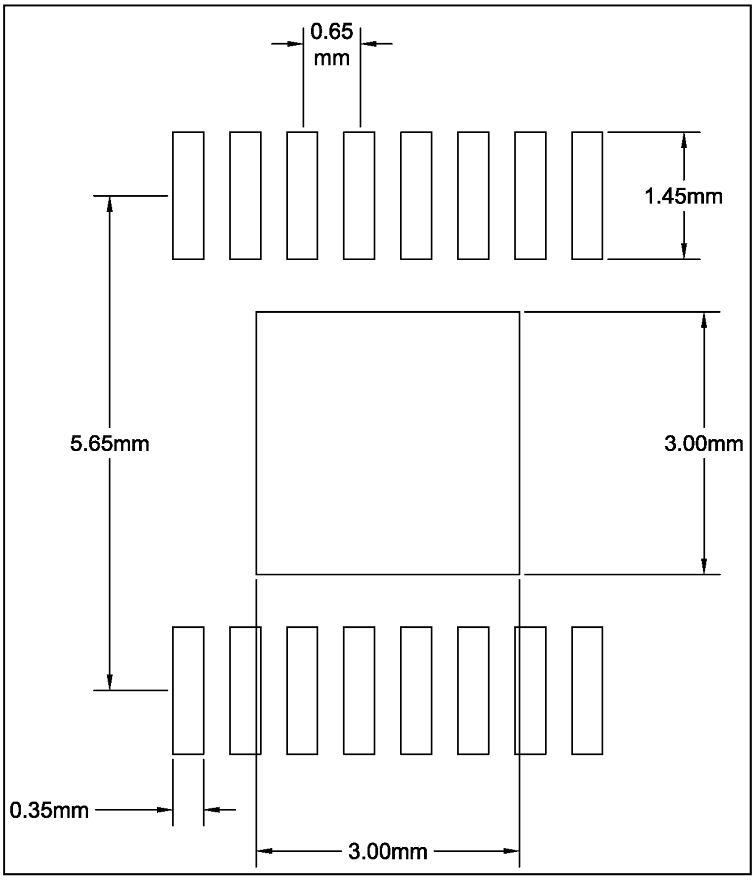
1)The thermal pad shows different shape among different factories.

2)Controlling dimension:mm

3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

eTSSOP-16



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2023.06.30
B	Update EC ΔI_{OUT_CH} limit value	2023.08.01
C	1. Update to new Lumissil logo 2. Update description about deglitch time 3. EC condition “T_A=T_J= ” changes to “T_J= ”	2024.05.08