

IS32LT3138A

18 CHANNELS LINEAR LED DRIVER WITH UART INTERFACE

January 2026

1 GENERAL DESCRIPTION

The IS32LT3138A is a linear programmable current regulator consisting of 18 output channels capable of up to 100mA each. UART communication interface compatible with CAN PHY is used for output control by a master microcontroller or ECU.

Each output can individually support 65536 steps PWM dimming and 128 steps DC current adjustment. The outputs can be combined to provide higher current drive capability to max 1.8A.

For added system reliability, the IS32LT3138A integrates fault detection circuitry for open/short string, single LED short, and over temperature conditions. The fault details can be got by interfaces. The fault pins (FAULTB) can all be tied together to disable the device and other IS32LT3138A devices on the same parallel circuit.

The IS32LT3138A is targeted at the automotive market such as interior accent lighting and exterior tail lighting. It is offered in WFQFN-32 (5mm×5mm) package.

2 APPLICATIONS

- Animation Rear Light
- Animation Tail Light
- Animation Daytime Running Light

3 SAFETY RELEVANT FEATURES

- LED open, single LED short and short detect via OP and comparator
- LDO voltage monitor via ADC and register
- PWM loop back test and loopback test BIST
- LBIST build in via LBIST
- Communication abnormal via communication watchdog timer
- Communication data error via CRC and checksum check
- VIN, LDO output Under voltage detection via comparator.

4 FEATURES

- Functional Safety-Capable
 - Developed according to ISO26262 with process complying to ASIL-B
- Wide input voltage supply from 4.5V to 16V
- Maximum output voltage 16V
- UART Communication Interface with LumiBus™ protocol
 - UART interface compatible with CAN physical layer, 1MHz maximum
 - UART communication with CRC to ensure robustness of communication
 - Support up to max. 64 addressable devices
 - Watch dog timer
 - Support Fail safe mode
- 18 channels capable of 100mA each
 - $\pm 2.5\%$ @ 100mA bit-to-bit current mismatch
 - $\pm 4\%$ @ 100mA device-to-device current accuracy
- Combined for higher current capability with same current accuracy
 - Minimum headroom voltage of 0.5V(Max.) at 100mA
- Individual PWM dimming to each channel
 - 65536 steps (16-bit) PWM duty cycle setting
 - 16-bit
 - 14+2-bit (with 2-bit dithering)
 - 13+3-bit (with 3-bit dithering)
 - 8+8-bit (with 8-bit dithering)
 - 8-bit
 - Phase delay minimizes inrush current-1 PWM base cycle (6 groups)
- Slew rate control and spread spectrum optimize EMI performance
- 64 steps global current setting
- Individual 128 steps DC current adjustment to each channel
- DC Binning support (ADJR pin)
- DC feedback for automatic DCDC VLED adjustment to optimize system power supply (DCFB)
- 10-Bit ADC for pin voltage measurement
- Support on OTP for data storage with fail safe mode1
- Fault protection with reporting
 - Fail safe modes selection
 - LED string open/short detect
 - Single LED short detect
 - Programmable fault reporting delay time
 - Programmable over temperature current roll off
 - Thermal shutdown
 - CRC error detection

IS32LT3138A

- Overcurrent (ISET pin short to GND)
- ISET pin open
- Fault pin pull down fault
- LED undervoltage
- PWM loop back detect
- SCA verification
- AEC-Q100 Qualified with Temperature Grade 1:
-40°C to 125°C
- Operating temperature range (-40°C ~ +125°C)
- WQFN-32 (5mm×5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

5 TYPICAL APPLICATION CIRCUIT

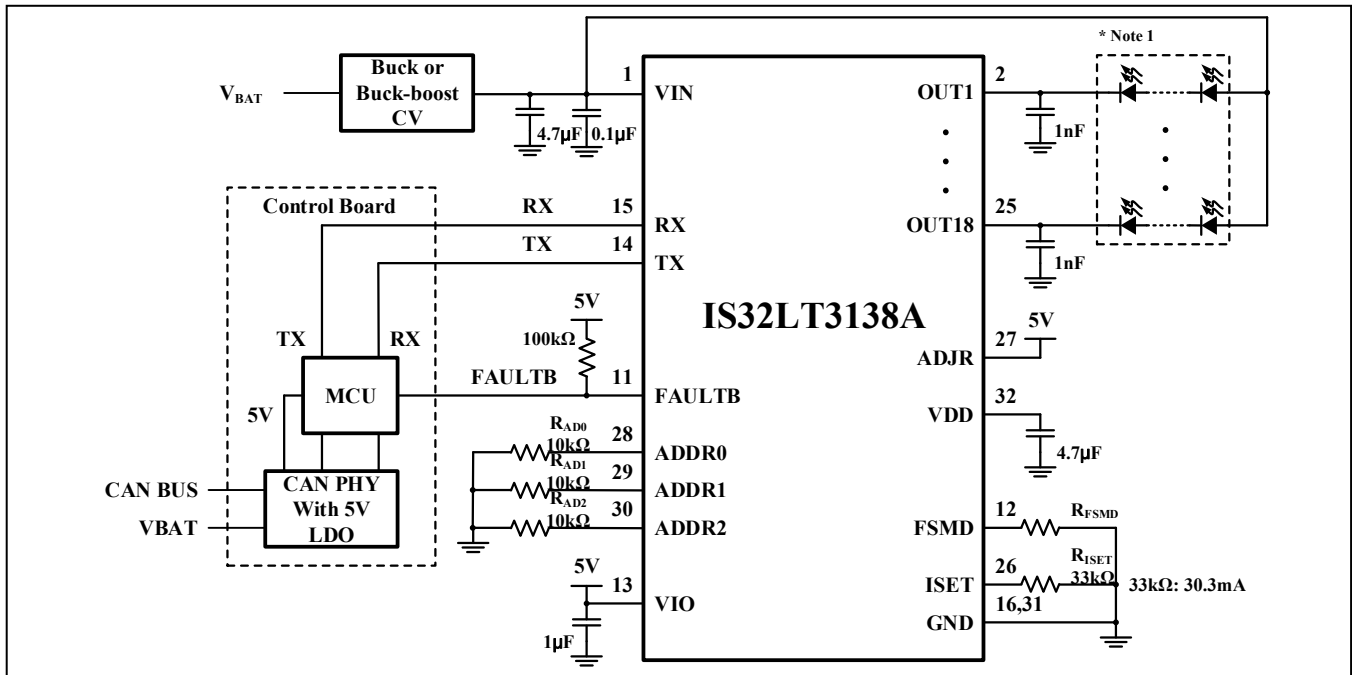


Figure 1 Typical Application Circuit of IS32LT3138A with UART Interface

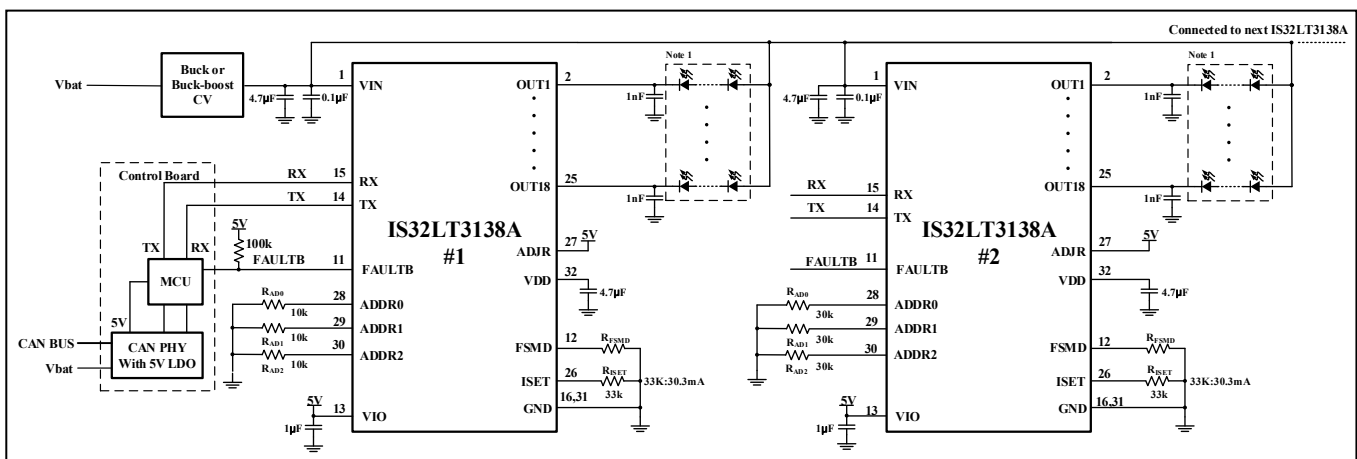


Figure 2 Typical Application Circuit of Several IS32LT3138A with UART Interface

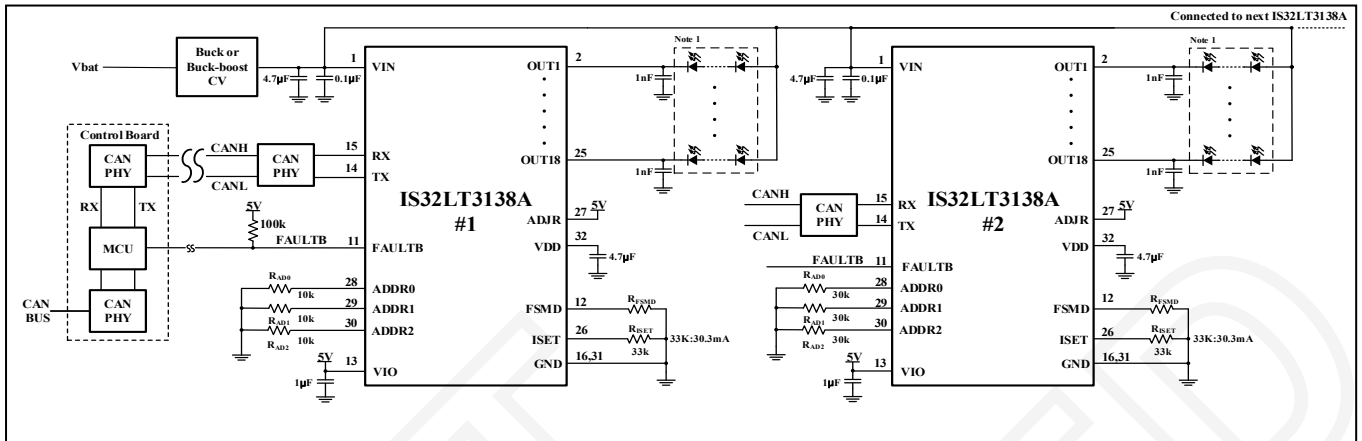


Figure 3 Typical Application Circuit of Multiple IS32LT3138A with External CAN Transceiver for Off-board Long Distance Communication

Note 1: The forward voltage variation of output LEDs should be kept as smaller as possible to minimize the heat consumption on device and prevent false fault triggering.

6 PIN CONFIGURATION

Package	Pin Configuration (Top View)
WFQFN-32	Pin Configuration (Top View) for WFQFN-32 package: - Top Row (Pins 1-8): VIN, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7 - Bottom Row (Pins 9-16): OUT8, OUT9, FAULTB, FSMD, VIO, TX, RX, GND - Right Side (Pins 17-24): OUT10, OUT11, OUT12, OUT13, OUT14, OUT15, OUT16/DCFB, OUT17/ADCIN1 - Left Side (Pins 25-32): OUT18/ADCIN2, ISET, ADJR, ADDR0, ADDR1, ADDR2, GND, VDD

PIN DESCRIPTION

No.	Pin	Description
1	VIN	Power supply input.
2~10, 17~25	OUT1~OUT18	Current sink channels.
11	FAULTB	Open drain fault reporting pin. In the “One Fail All Fail” mode, this pin also is an input pin. Pulling this pin low will disable the outputs.
12	FSMD	Connect different resistor to GND to select fail safe mode.
13	VIO	For TX power supply.
14	TX	UART interface transmitted data pin.
15	RX	UART interface received data pin.
16, 31	GND	Ground.
23	OUT16/ DCFB	DC feedback for automatic DCDC VLED adjustment to optimize system power supply.
24	OUT17/ ADCIN1	ADC input.
25	OUT18/ ADCIN2	ADC input.
26	ISET	Input pin used to connect an external resistor to set the global output current.
27	ADJR	For analog dimming control.
28~30	ADDR0~ADDR2	Address setting. Connect a resistor from this pin to GND to assign the address.
32	VDD	4.2V LDO output. Connect a 4.7 μ F X7R capacitor to GND.
	Thermal Pad	Must be connected to GND. Connect thermal pad to external GND plane on board for better thermal performance.

IS32LT3138A



7 ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3138A-QWLA3-TR IS32LT3138A-QWLCA3-TR (Note 2)	WFQFN-32, Lead-free	2500

Note 2: IS32LT3138A-QWLCA3-TR is with copper wire bonding.

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

8 SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{IN}	-0.3V ~ 20.0V
Voltage at TX, RX, ADDR _x , ISET, VDD, VIO, ADJR, FSMD	-0.3V ~ 6V
Voltage at OUT1 to OUT18, FAULTB	+20V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, $T_A=T_J$	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	38.2°C/W
Package thermal resistance, junction to case (bottom) (4-layer standard test PCB based on JESD 51-14), θ_{JC_BOT}	10.1°C/W
ESD (HBM)	±2.5kV
ESD (CDM)	±750V

Note 3: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 ELECTRICAL CHARACTERISTICS

$V_{IN}=12V$, $T_J=-40^{\circ}C \sim 125^{\circ}C$, unless otherwise noted. (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage		4.5		16	V
I_{OUT}	Maximum output current	$R_{ISET}=10k\Omega$, $GCC=0x3F$, $SCAx=0x7F$, $PWM=0xFFFF$	95	100	105	mA
	Output current	$R_{ISET}=33k\Omega$, $GCC=0x3F$, $SCAx=0x7F$, $PWM=0xFFFF$	28.5	30.3	31.5	mA
ΔI_{MAT}	I_{OUT} mismatch (bit to bit) (Note 4)	$I_{OUT}=30.3mA$	-2.5		2.5	%
		$I_{OUT}=100mA$	-2.5		2.5	%
ΔI_{OUT}	I_{OUT} accuracy (device to device) (Note 5)	$I_{OUT}=30.3mA$	-3		3	%
		$I_{OUT}=100mA$	-4		4	%
V_{HR}	Headroom voltage	$I_{OUT}=100mA$		0.34	0.5	V
		$I_{OUT}=30.3mA$		0.2	0.4	V
I_{CC}	Quiescent power supply current	$R_{ISET}=33k\Omega$, $GCC=0x3F$, $SCAx=0x7F$, $PWM=0$	4	5.49	7.5	mA
V_{ISET}	ISET voltage	$R_{ISET}=10k\Omega$, $GCC=0x3F$, $SCAx=0x7F$, $PWM=0xFFFF$	1.94	2.0	2.06	V
I_{OZ}	Output leakage current	$I_{OUT}=0$, $V_{OUT}=16V$			1	μA
f_{OUT}	PWM frequency of output	Frequency setting=31kHz, 8bit PWM mode	27.9	31	34.1	kHz
		Frequency setting=122Hz, 16bit PWM mode	109.8	122	134.2	Hz
T_{SD}	Thermal shutdown			168		°C
T_{SD_HYS}	Thermal shutdown hysteresis			15		°C

8.3 ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted. (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{PD_FAULTB}	FAULTB pin pull-down capability	I _{SINK} = 2mA		0.1	0.2	V
I _{LKG_FAULTB}	FAULTB pin leakage current	V _{PULL-UP} = 16V			2	μA
V _{IH_FAULTB}	FAULTB pin high-level input voltage	Fault action mode is set to "One Fail All Fail"(OFA [1:0] ≠ 11) (Note 7)	2.4			V
V _{IL_FAULTB}	FAULTB pin low-level input voltage	Fault action mode is set to "One Fail All Fail"(OFA [1:0] ≠ 11) (Note 7)			0.7	V
V _{IH_RX}	Logic "1" input voltage		2			V
V _{IL_RX}	Logic "0" input voltage				0.7	V
V _{OL(TX)}	LOW level output voltage	I _{SINK} = 5mA			0.3	V
V _{OH(TX)}	High level output voltage	I _{SOURCE} =5mA	V _{IO} -0.3		V _{IO}	V
V _{T1_AD/FS}	ADDR0/ADDR1/ADDR2/FSMD threshold1		0.9	1	1.1	V
V _{T2_AD/FS}	ADDR0/ADDR1/ ADDR2/FSMD threshold2		1.85	2	2.15	V
V _{T3_AD/FS}	ADDR0/ADDR1/ ADDR2/FSMD threshold3		2.8	3	3.2	V
I _{AD/FS}	ADDR/FS source current		46	50	54	μA
V _{SC_FL}	LED string short detection falling threshold	R _{ISSET} =33kΩ, GCC= 0x3F, SCAx= 0x7F, PWM=0xFFFF, measured at VIN-OUTx SHORT_FLT(43h) = "000"	0.5	1		V
V _{SC_RS}	LED string short detection rising threshold	R _{ISSET} =33kΩ, GCC= 0x3F, SCAx = 0x7F, PWM=0xFFFF, measured at VIN-OUTx SHORT_FLT(43h) = "000"		1.2		V
V _{OC_FL}	LED string open detection falling threshold	R _{ISSET} =33kΩ, GCC= 0x3F, SCAx = 0x7F, PWM=0xFFFF, measured at OUTx	50	100		mV
V _{OC_RS}	LED string open detection rising threshold	R _{ISSET} =33kΩ, GCC= 0x3F, SCAx = 0x7F, PWM=0xFFFF, measured at OUTx		180		mV
V _{DD}	LDOOUT output voltage		4.08	4.2	4.32	V
I _{DD_MAX}	LDOOUT output current capability	V _{IN} > 4.5V, V _{DD} >3.8V			50	mA
I _{DD_LIM}	LDOOUT output current limit	V _{IN} =12V, V _{DD} =0V	60			mA
V _{DD_UV}	LDOOUT undervoltage-lockout threshold	Voltage falling, IC disabled		3.7		V
V _{DD_UVHY}	VDD undervoltage-lockout hysteresis			100		mV
ΔI _{CTRL}	IOUT mismatch (bit to bit)	V _{ADJ} ×30%, V _{ADJ} = 2V	-3		3	%
ΔI _{CTRL}		V _{ADJ} ×70%, V _{ADJ} = 2V	-3		3	%
V _{SLSH}	Single LED short detect threshold	SLSTH (39h~41h) = "0010"		3.9		V

8.4 ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted. (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{F_UVLO}	LED short/OPEN UVLO	FS_FLTL (43h) = "00000100"		8		V
V _{IO}	TX/MISO power supply		3		5.5	V
V _{VIN_UV}	VIN undervoltage-lockout threshold	Voltage falling, IC disable		3.7		V
V _{VIN_UVHY}	VIN undervoltage-lockout hysteresis			100		mV
f _{OSC}	System clock frequency		32.34	33	33.66	MHz
ADC (10-bit)						
V _{REFADC}	Reference voltage		2.43	2.5	2.57	V
DNL	Differential nonlinearity	(Note 6)	-5		+5	LSB
INL	Integral nonlinearity	(Note 6)	-8		+8	LSB
RESADC	Quantization steps		1024			LSB
ADCERR	Quantification error		-0.5		+0.5	LSB
t _{CONV}	Min. conversion time	For max. ADC input frequency = 1MHz (Note 7)		25		μs

Note 4: I_{OUT} mismatch (bit to bit) ΔI_{MAT} is calculated:

$$\Delta I_{MAT} = \max \left(\left| \frac{I_{OUTn}(n = 1 \sim 18)}{I_{OUT1} + I_{OUT2} + \dots + I_{OUT18}} - 1 \right| \right) \times 100\%$$

Note 5: I_{OUT} accuracy (device to device) ΔI_{OUT} is calculated:

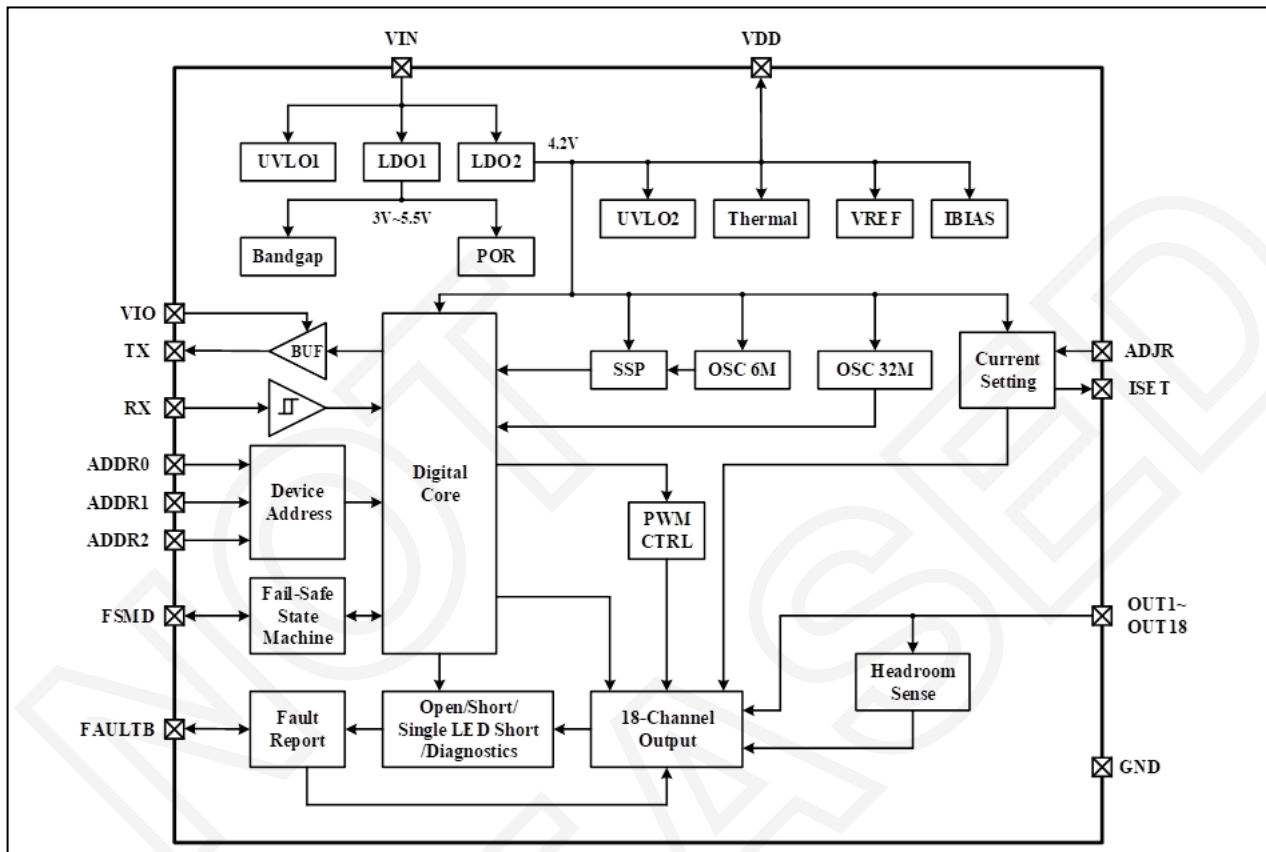
$$\Delta I_{OUT} = \left| \frac{I_{OUT1} + I_{OUT2} + \dots + I_{OUT18}}{18} - I_{OUT(TYP)} \right| \times 100\%$$

When R_{ISSET}= 10kΩ, I_{OUT(TYP)}= 100mA; and when R_{ISSET}= 33kΩ, I_{OUT(TYP)}= 30mA.

Note 6: Production testing of the device is performed at 25°C.

Note 7: Guaranteed by design.

9 FUNCTIONAL BLOCK DIAGRAM



10 APPLICATION INFORMATION

10.1 OVERVIEW

The IS32LT3138A is a linear programmable current regulator consisting of 18 output channels capable of up to 100mA each. UART communication interface compatible with CAN PHY is used for output control by a master microcontroller or ECU. Each output can individually support 65536 steps PWM dimming and 128 steps DC current adjustment. The outputs can be combined to provide higher current drive capability to max 1.8A.

For added system reliability, the IS32LT3138A features various fault protections, including LED string open/short, single LED short, overcurrent (ISET shorted), ISET pin opened, PWM duty verification fail, SCA verification fail, Thermal Rolloff, Thermal shutdown, external (One Fail All Fail modes), CRC error and watchdog 1 or watchdog 2 timeout (fail-safe modes) conditions for robust operation. The detection of these failures is reported by a dedicated reporting pin, FAULTB. There are also dedicated flag bits in registers for each failure which can be read back by the external host MCU through the interfaces. To optimize EMI performance, the IS32LT3138A features spread spectrum on the internal PWM base clock to spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. In addition, the output current source ON/OFF transitions during PWM dimming have a slow rate control and programmable phase delay to mitigate EMI and power supply inrush current.

The IS32LT3138A interface is UART, and it supports up to 64 slave IS32LT3138A devices. The device address can be configured by the three address pins. The UART receives data to control all output channels and sends back fault information to the host MCU. The UART interface in conjunction with an external standard CAN transceiver enables long distance communication with a host MCU placed outside of the lamp module (as shown in Figure 4). Based on the CAN physical layer, it achieves excellent EMC and EMI performance. The embedded CRC correction of the UART data stream can ensure robust communication in automotive environments. The UART interface is easily supported by most MCUs in the market.

To further increase robustness, the fail-safe mode of the device allows automatic switching to fail-safe state in case of the communication loss, for example, host MCU failure or communication cables broken. The device supports different fail-safe modes configured by the FSMD pin.

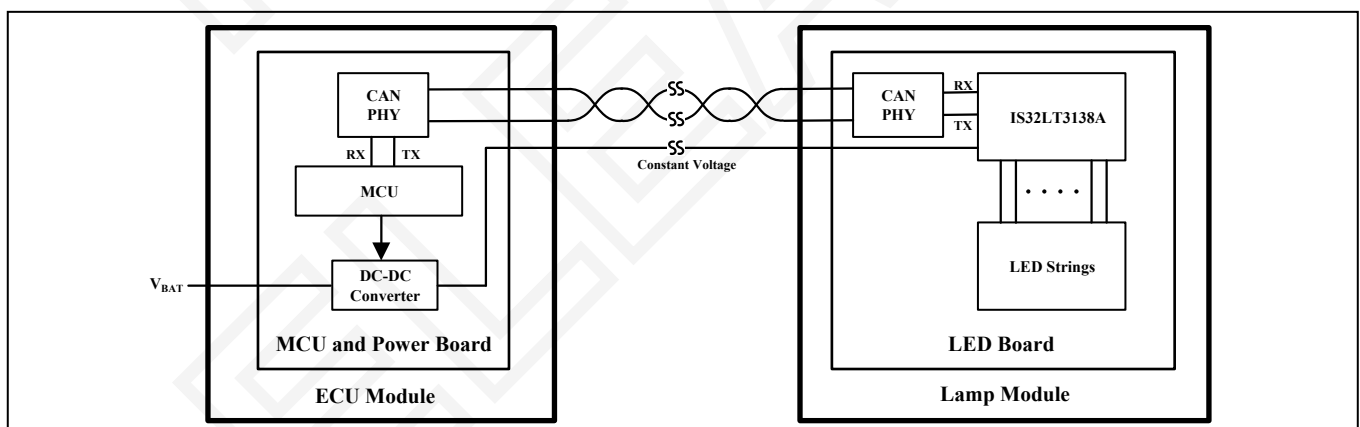


Figure 4 UART Interface with External CAN Transceiver for Outside Module Long Distance Communication

10.2 POWER SUPPLY

10.2.1 VIN UNDERVOLTAGE-LOCKOUT (UVLO)

The IS32LT3138A features an undervoltage-lockout (UVLO) function on the VIN pin to prevent unintended operation at too low supply voltages. UVLO threshold is an internally fixed value and cannot be adjusted. Entering UVLO will reset all registers to their default value. The device is disabled when the VIN voltage drops below V_{VIN_UV} and automatically resumes normal operation when the VIN voltage rises above $(V_{VIN_UV} + V_{VIN_UVHY})$.

10.2.2 INTERNAL 4.2V LINEAR REGULATOR (VDD)

The IS32LT3138A device integrates an internal linear regulator (LDO) with 4.2V (Typ.) and I_{DD_MAX} current capability to provide power supply to the internal analog and digital circuits. During operation, the internal circuitry can be subject to transient currents from this linear regulator. Therefore, a 4.7μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND, it must be placed as close to the VDD pin as possible. This linear regulator also has the UVLO feature. The device is disabled when the V_{DD} voltage drops below V_{DD_UV} and resumes normal

operation when the VDD voltage rises above (V_{DD_UV}). Entering UVLO will reset all registers to their default value. An I_{DD_LIM} current limit on VDD pin protects the IS32LT3138A from VDD output overload or short-circuit conditions.

10.2.3 VIO VOLTAGE SUPPLY

The positive voltage rail of the UART interface is supplied with the VIO pin which must be connected to a proper voltage source. Usually, the VIO pin should be connected to the same power supply as the MCU. If a 5V MCU is used for IS32LT3138A control, the VIO pin can be directly connected to the VDD pin.

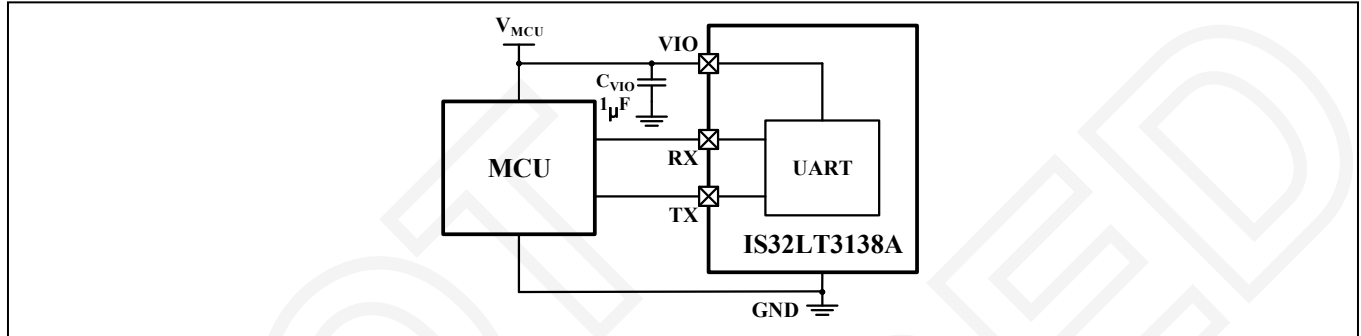


Figure 5 VIO Voltage Supply

10.3 OUTPUT CURRENT SETTING

The full DC output current (I_{OUT_FU}) for each channel is set with resistor (R_{ISET}) connected from the ISET pin to GND. This current set resistor is computed using the following equation:

$$I_{OUT_FU} = \frac{V_{ISET}}{R_{ISET}} \times 500 \quad (1)$$

Where V_{ISET} is the voltage of ISET pin, when V_{ADJ} is lower than 2V (typ.),

$$I_{OUT_FU} = \frac{V_{ADJ}}{R_{ISET}} \times 500 \quad (2)$$

($10k\Omega \leq R_{ISET} \leq 75k\Omega$)

It is recommended that R_{ISET} be a 1% accuracy resistor with good temperature characteristic to ensure stable output current. R_{ISET} must be placed as close to ISET pin as possible on PCB layout to avoid noise interference and ground bounce. The device is protected from an output overcurrent condition caused by R_{ISET} resistor. The output current is reduced to 17mA (Typ.) if the ISET pin is shorted to ground or R_{ISET} resistor value is too low.

When R_{ISET} is fixed, the DC output current for each channel can be further adjusted in 64-steps by the GCC[5:0] bits in the GC_CTRL register (01h). Furthermore, based on the GCC[5:0] setting, each channel also supports individual 128-step programmable DC output current adjustment. This feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on an external visual calibration system to further save binning cost. The 7-bit Scaling Registers SCAX (03h~14h) individually set the DC output current of each channel.

GCC[5:0] and SCAX control the OUTx current (I_{OUTx}) as shown in following equation:

$$I_{OUTx} = I_{OUT_FU} \times \frac{GCC}{63} \times \frac{SCAx}{127} \quad (3)$$

Where x is from 1 to 18 for different output channel.

$$GCC = \sum_{n=0}^5 D[n] \cdot 2^n \quad (4)$$

$$SCAx = \sum_{n=0}^6 D[n] \cdot 2^n \quad (5)$$

For example: assume GCC[5:0] = 0x05 and SCA1 = 0x40. GCC = 5. Then the DC output current of OUT1 is:

$$I_{OUT1} = I_{OUT_FU} \times \frac{5}{63} \times \frac{64}{127}$$

If any channel(s) are unused, please connect the corresponding OUTx pin(s) to the GND pin to avoid false fault detection and set the corresponding PWM and scaling registers to "0x00" to turn off these output(s).

10.4 ANALOG DIMMING

The IS32LT3138A offers an analog dimming input pin, ADJR. The dimming voltage range of ADJR pin is 0.06V to 2V. The global output current can be regulated by the ADJR pin voltage. If the analog dimming pin ADJR is pulled up above 2V, analog dimming is disabled, and the output current is 100% (full current). When the ADJR pin is driven below 2V, the analog dimming is enabled, and the pin voltage (0.06~2V) will proportionally control the output current.

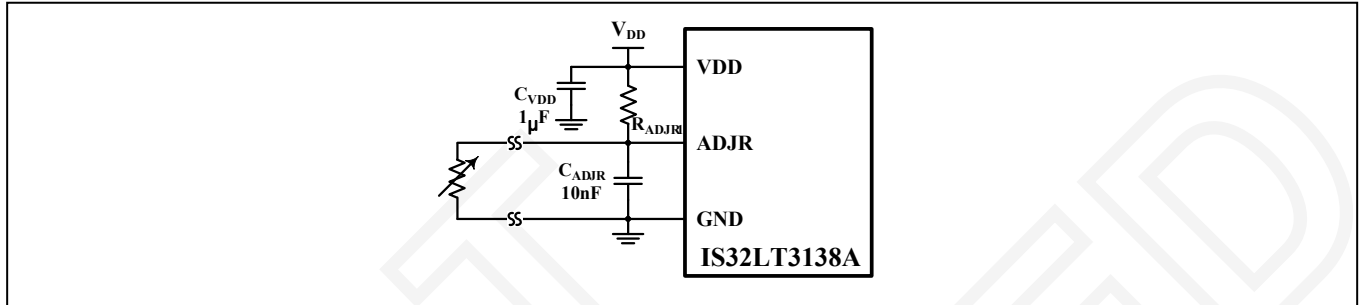


Figure 6 IS32LT3138A Analog Dimming for LED Binning

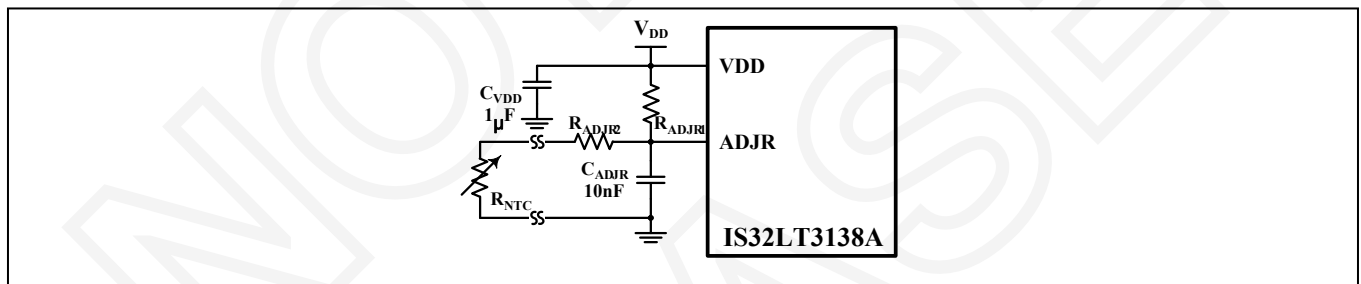


Figure 7 IS32LT3138A Analog Dimming for Thermal Roll-off

The ADJR pin can be used to fine tune the output current for LED binning during mass-production. The ADJR pin can also be used in conjunction with an NTC thermistor to provide over temperature current roll-off protection for the LED load or the system. As shown in Figure 6 and Figure 7, the IS32LT3138A can perform either LED binning or thermal roll-off function, not both at the same time.

10.5 PWM DIMMING

The IS32LT3138A integrates independent 16-bit PWM generators for each output channel. The output current for each channel is turned on and off as controlled by the PWM generator. The average current of each output channel can be adjusted by its PWM duty cycle to control the LED channel brightness. The PWM Registers (15h~38h) individually set the PWM duty cycle for each channel.

The PWM dimming frequency is programmable by the CONFIG register (00h). The maximum PWM frequency can be up to 31kHz (typ.). Due to the output current slew rate control, a high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio. At a 100Hz~1000Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower. Select the PWM dimming frequency based on the minimum brightness requirement for the application.

The PWM generators dim the LEDs by their duty cycle:

$$I_{OUTx_PWM} = I_{OUTx} \times D_{PWMx} \quad (6)$$

Where D_{PWMx} is the duty cycle of each channel independently programmed by PWM Registers (15h~38h), in 16bit or 8+8-bit PWM mode or 13+3-bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{15} D[n] \cdot 2^n}{65536} \quad (7)$$

In 8bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=8}^{15} D[n] \cdot 2^n}{256} \quad (8)$$

10.5.1 PWM SPREAD SPECTRUM

The IS32LT3138A includes a spread spectrum feature on PWM base clock to optimize EMI performance. The spread spectrum function helps spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. With spread spectrum, the EMI test can be passed with smaller size and lower cost filter circuit. Spread spectrum is enabled/disabled by the SYSCFG register (42h).

10.5.2 PWM PHASE DELAY

To mitigate transient current generation and power supply ripple, the IS32LT3138A features PWM phase delay. When PWM phase delay is disabled (PDE (00h) is set to "0", default value is "1" phase delay enables), all channels are simultaneously turned on at the beginning of each PWM cycle. This will result in large current draw from power supply leading to high voltage ripple on the power supply rail. As shown in figure 8.

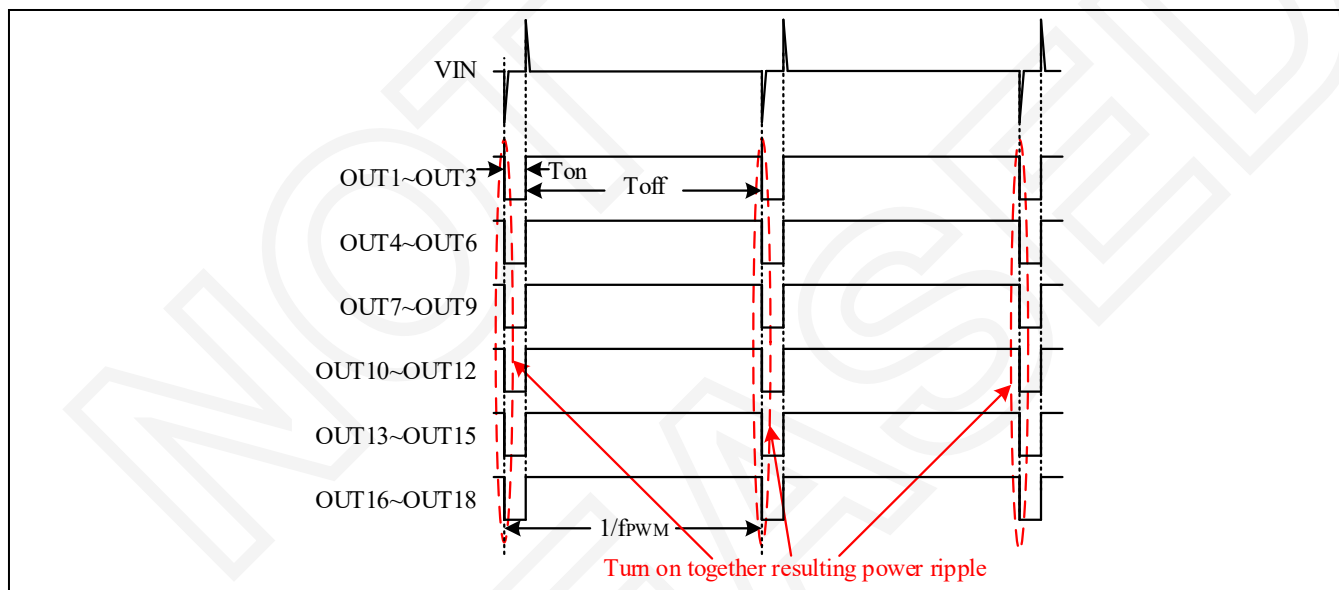


Figure 8 PWM Phase Delay Disabled

The IS32LT3138A divides 18 output channels into 6 groups to perform PWM phase delay, OUT1&OUT2&OUT3 as group 1, OUT4&OUT5&OUT6 as group 2, ... OUT16&OUT17&OUT18 as group 6. When the PDE bit in the CONFIG register (00h) is set to "1", the phase delay is enabled, starting each group in turn from each PWM cycle. The t_{DELAY_1} is interval delay time between group n & group n+1, and t_{DELAY_1} is 1/6 PWM cycle ($1/f_{\text{PWM}}$). This minimizes the voltage ripple on the VIN power supply rail. As shown in figure 9.

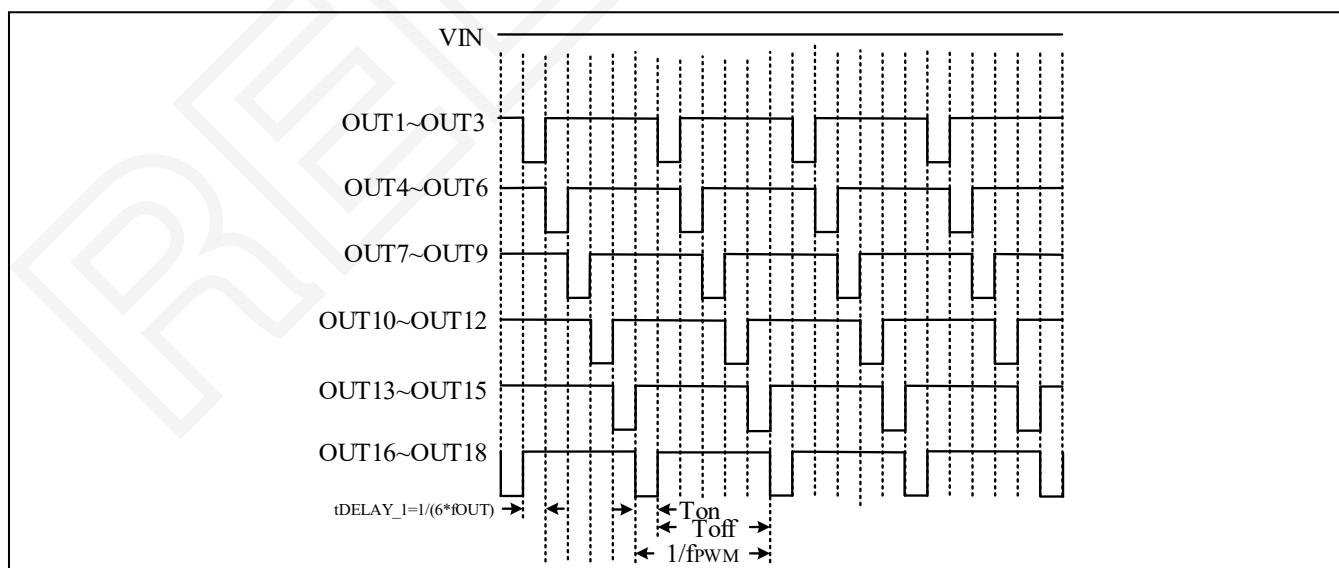


Figure 9 PWM Phase Delay Enabled

10.6 FAULT PROTECTION

10.6.1 FAULT REPORTING

For added system reliability, the IS32LT3138A integrates various fault detections for LED string open/short, single LED short, overcurrent (ISET shorted), ISET pin opened, PWM duty verification fail, SCA verification fail, Thermal Rolloff, Thermal shutdown, external (One Fail All Fail modes), CRC error and watchdog 1 or watchdog 2 timeout (fail-safe modes) conditions. The open drain pin FAULTB can be used for fault condition reporting. If any fault occurs, the corresponding bit in FLT_TYPE register will be set to “1” and the FAULTB pin will go low after a delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report fault condition. When it's monitored by a host MCU, a pull-up resistor R_{FPU} (10kΩ recommended) from the FAULTB pin to the supply of the host MCU is required.

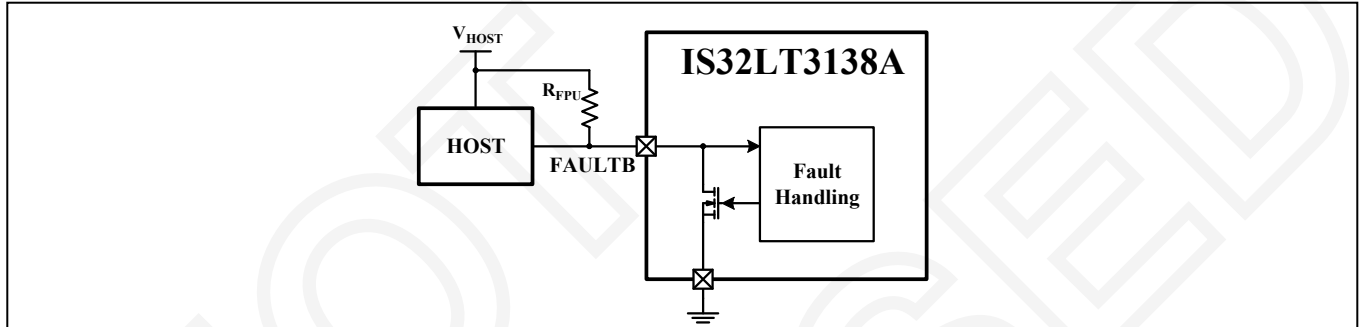


Figure 10 Host Monitors the Fault Reporting

10.6.2 LED STRING OPEN PROTECTION

The LED string open detection is enabled by setting the ODE and ODF bits in FLT_DET_EN register (44h) to “1”. If any LED string is opened, the corresponding OUTx pin voltage will be pulled down close to zero. When the OUTx pin voltage, V_{OUTx} , falls below the LED string open detection voltage, V_{OC_FL} and persists for longer than a deglitch time (typical 10μs), the LED string open protection will be triggered. The corresponding fault flag bits in OPEN_FLT register (49h & 4Ah & 4Bh) and the OPENF bit in FAULT_TYPE_2 register (51h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device will recover to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) expires once the open condition is removed, i.e. V_{OUTx} rising above the LED string open detection voltage, V_{OC_RS} . The corresponding fault flag bit in OPEN_FLT register will reset to “0”. However, the OPENF bit in FAULT_TYPE_2 register (51h) is latched, which means that it cannot automatically reset to “0” after open condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string open detection is only enabled during the PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string open fault.

10.6.3 LED STRING SHORT PROTECTION

The LED string short detection is enabled by setting the SDE and SDF bits in FLT_DET_EN register (44h) to “1”. If any LED string is short, the corresponding OUTx pin will be pulled up close to V_{IN} . When dropout voltage from the V_{IN} pin to the OUTx pin, $V_{IN}-V_{OUTx}$ (when SHORT_FLT(43h) = “000”), rises above the LED string short detection voltage, V_{SC_RS} , and persists for longer than a deglitch time (typical 10μs), the LED string short protection will be triggered. The corresponding fault flag bits in SHORT_FLT register (46h & 47 & 48h) and the SHORTF bit in FAULT_TYPE_2 register (51h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the short condition is removed, V_{OUTx} falling above the LED string short detection voltage, V_{SC_FL} . The corresponding fault flag bit in SHORT_FLT register will reset to “0”. However, the SHORTF bit in FAULT_TYPE_2 register (51h) is latched, which means that it cannot automatically reset to “0” after short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string short fault.

When the device is operated in DC mode, the PWM function is disabled. It is recommended to not enable both LED string short and single LED short, because the IS32LT3138A may incorrectly report an LED string short as a single LED short. Individually enable either LED string short or single LED short detection. If a single LED short is reported, double check for LED string short or single LED short in software.

10.6.4 SINGLE LED SHORT PROTECTION

The single LED short detection is enabled by setting the SLSDE and SLSDF bits in FLT_DET_EN register (44h) to "1". Then the single LED short detection is active after VIN voltage rising above the fault undervoltage-lockout voltage threshold V_{FLT_UV} . That helps to prevent false fault detection due to the insufficient power supply voltage, such as power up transience. The single LED short detect threshold V_{SLSTH} of each channel is individually programmed by the corresponding LEDx_SLS[4:0] bits in LEDx_SLSTH registers (39h~41h). If single LED of any string is shorted, the corresponding OUTx pin voltage will rise. When the OUTx pin voltage, V_{OUTx} , rise above single LED short detect threshold, V_{SLSTH} , and persists for longer than a deglitch time (typical 10 μ s), the single LED short protection will be triggered. The corresponding fault flag bits in SLS_FLT register (4Ch & 4Dh & 4Eh) and the SLS_FLT bit in FAULT_TYPE_2 register (51h) will be set to "1". The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

The device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the single LED short condition is removed, V_{OUTx} rising above the LED string short detection voltage, V_{SLSTH} . The corresponding fault flag bit in SLS_FLT register will reset to "0". However, the SLSHORTF bit in FAULT_TYPE_2 register (51h) is latched, which means that it cannot automatically reset to "0" after single LED short condition being removed but must be cleared by the host MCU writing it back to "0".

When PWM dimming is implemented, the single LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10 μ s), the device does not report any single LED short fault.

10.6.5 OUTPUT OVERCURRENT (ISET PIN SHORT)

The device is protected from an output overcurrent condition caused by the Riset resistor. All output current is limited to 110mA (Typ.) in case the ISET pin shorted to ground or too low value Riset resistor is connected to ISET pin. If the condition persists for longer than a deglitch time (typical 1 μ s), the ISET pin short protection will be triggered. All output current will be reduced to 17mA (Typ.). If the RSET_SHE bit in FAULT_EN register (4Fh) is set to 1, the RSET_SH bit in FAULT_TYPE_1 register (50h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the RSET_SH bit in FAULT_TYP_1 register (50h) is latched, which means that it cannot automatically reset to "0" after ISET short condition being removed but must be cleared by the host MCU writing it back to "0".

10.6.6 ISET PIN OPEN

In case of the ISET pin open or too High value Riset resistor is connected to ISET pin. If the condition persists for longer than a deglitch time (typical 1 μ s), the ISET pin open protection will be triggered. If the RSET_OPE bit in FAULT_EN register (4Fh) is set to 1, the RSET_OP bit in FAULT_TYPE_1 register (50h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the RSET_OP bit in FAULT_TYP_1 register (50h) is latched, which means that it cannot automatically reset to "0" after ISET open condition being removed but must be cleared by the host MCU writing it back to "0".

10.6.7 EXTERNAL FAULT

External fault is to achieve the One Fail All Fail function, multiple IS32LT3138A applications by connecting the FAULTB pins of each IS32LT3138A in parallel, And set the OFA[1:0] bit of CONFIG register (00h) to One Fail All Fail, When FAULTB pins are pulled down externally persists for longer than a deglitch time, the EXF bit in FAULT_TYPE_2 register (51h) will be set to "1".

FAULT_TYP_2 register (51h) is latched, which means that it cannot automatically reset to "0" after External fault condition being removed but must be cleared by the host MCU writing it back to "0".

10.6.8 SCA VERIFICATION

SCA verification fault is enabled by opening the SCAF_EN bit in the FLT_DET_EN register (44h) to "1". Any output SCA verification failure occurs, the SCAVF bit in FAULT_TYPE_2 register (51h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

FAULT_TYP_2 register (51h) is latched, which means that it cannot automatically reset to "0" Even if Disabled SCA verification function but must be cleared by the host MCU writing it back to "0".

10.6.9 PWM DUTY VERIFICATION

PWM duty verification fault is enabled by opening the DUTYF_EN bit in the FLT_DET_EN register (44h) to "1". Any output occurs loopback verification failure, the LPBF bit in FAULT_TYPE_2 register (51h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

FAULT_TYP_2 register (51h) is latched, must be cleared by the host MCU writing it back to "0", For the LPBF bit, the MODE[1:0] bit of the VFYCTL register (91h) must be set to 00(Disabled loop back) to clear the LPBF bit of the FAULT_TYP_2 register (51h).

10.6.10 THERMAL SHUTDOWN

If the junction temperature exceeds TSD (Typ. 168°C), all output channels will go to the OFF state and the TSD bit in FAULT_TYPE_1 register (50h) will be set to "1". If the TSDE bit in FAULT_EN register (4Fh) to "1", the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. At this point, the device presumably begins to cool off. Any attempt to toggle the channels back to the source condition before the device has cooled to below ($T_{SD}-T_{SD_HYS}$) (Typ. 155°C) will be blocked and the device will not be allowed to restart. The FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the device cools down. However, the TSD bit in FAULT_TYPE_1 register (50h) is latched, which means that it cannot automatically reset to "0" but must be cleared by the host MCU writing it back to "0".

10.6.11 THERMAL ROLL-OFF PROTECTION

The device integrates the thermal shutdown protection to prevent the device from overheating. In addition, to prevent the LEDs from flickering due to rapid thermal changes, the device also includes a programmable thermal roll-off feature to reduce power dissipation at high junction temperature.

The current output will be equal to the set value I_{OUTx} if the junction temperature of the device remains below thermal roll-off temperature threshold 120°C. If the junction temperature exceeds the temperature threshold, the output current of all channels will begin to linearly reduce following the junction temperature ramping up until thermal shutdown. The TF bit in FAULT_TYPE_1 register (50h) will be set to "1". If the TFE bit in FAULT_EN register (4Fh) to "1", the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The percentage of the current output before thermal shutdown is programmable by the TROF[2:0] bits in the TEMP_SEN register (02h).

The current output will linearly resume to the set value I_{OUTx} and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the junction temperature cools down below the thermal roll-off temperature threshold 120°C. However, the TF bit in FAULT_TYPE_1 register (50h) is latched, which means that it cannot automatically reset to "0" but must be cleared by the host MCU writing it back to "0".

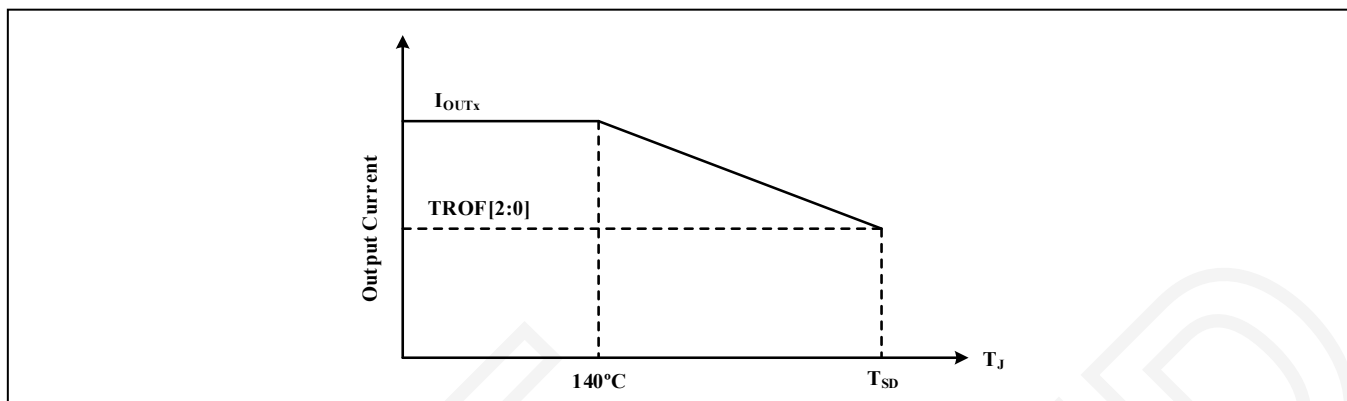


Figure 11 Thermal Roll-off Protection

By mounting the IS32LT3138A device on the same thermal substrate as the LEDs, use of this feature can also limit the dissipation of the LEDs.

10.6.12 FAULT ACTION TABLE

Fault Action Table (Both Normal State and Fail-Safe State)

Fault Type	Detection	Conditions	Actions	Fault Flags	FAULTB Pin	Recovery
Supply UVLO	$V_{IN} < V_{VIN_UV}$ or $V_{DD} < V_{DD_UV}$	-	Turn off all channels and reset all registers to default value	-	No action	$V_{IN} > (V_{VIN_UV} + V_{VIN_UVHY})$ or $V_{DD} > (V_{DD_UV} + V_{DD_UVHY})$
LED string open	$V_{IN} > V_{FLT_UV}$ and $V_{OUTx} < V_{OC_FL}$	PWM pulse width greater than 10 μ s (Typ.) and ODE = 1	Faulty channel outputs 4mA and other channels on (ODF = 1)	OPEN_FLT and OPENF bit	Pull low (ODF = 1)	$V_{OUTx} > V_{OC_RS}$ Write OPENF bit to "0"
LED string short	$(V_{IN} - V_{OUTx}) < V_{SC_RS}$ (SHORT_FLT=000) or $V_{OUTx} > V_{SC}$ (SHORT_FLT#000)	PWM pulse width greater than 10 μ s (Typ.) and SDE = 1	Faulty channel outputs 4mA and other channels on (SDF = 1)	SHORT_FLT and SHORTF bit	Pull low (SDF = 1)	$(V_{IN} - V_{OUTx}) > V_{SC_FL}$ (SHORT_FLT=000) or $V_{OUTx} < V_{SC}$ (SHORT_FLT#000) Write SHORTF bit to "0"
Single LED short	$V_{IN} > V_{FLT_UV}$ and $V_{OUTx} > V_{SLSTH}$	PWM pulse width greater than 10 μ s (Typ.) and SLSDE = 1	Faulty channel outputs 4mA and other channels on (SLSDF = 1)	SLST_FLT and SLSHORTF bit	Pull low (SLSDF = 1)	$V_{OUTx} < V_{SLSTH}$ Write SLSHORTF bit to "0"
ISET pin short (Overcurrent)	I_{OUTx} limited to 110mA (Typ.)	Longer than 1 μ s (Typ.) deglitch time and RSET_OPE = 1	All channels reduced to 17mA (Typ.)	RSET_SH bit	Pull low	ISET pin to GND resistance resumes to normal range, Write RSET_SH bit to "0"
ISET pin open	ISET pin open	Longer than 1 μ s (Typ.) deglitch time and RSET_SHE = 1	-	RSET_OP bit	Pull low	ISET pin to GND resistance resumes to normal range, Write RSET_SH bit to "0"
External fault	FAULTB pins are pulled down	OFA [1:0] $\neq$ 11	All channels off	EXF bit	-	FAULTB pins are pull up Write EXF bit to "0"
SCA verification	Any output occurs SCA verification failure	-	-	SCAVF bit	Pull low (SCAF_EN = 1)	Write SCAVF bit to "0"
PWM duty verification	Any output occurs PWM duty verification failure	-	-	LPBF bit	Pull low (DUTYF_EN = 1)	Disabled loop back, Write DUTYF_EN bit to "0"
Thermal shutdown	$T_J > T_{SD}$	-	All channels off	TSD bit	Pull low (TSDE = 1)	$T_J < (T_{SD} - T_{SD_HYS})$ Write TSD bit to "0"
Thermal roll-off	$T_J > 120^\circ\text{C}$	TROF[2:0] $\neq$ 00	All channels linearly reduce output current	TF bit	Pull low (TFE = 1)	$T_J < 120^\circ\text{C}$ Write TF bit to "0"
CRC error	Calculated CRC does not match CRC data	-	Increments CRC Error Count register	CRCF bit	Pull low	Write CRCF bit to "0"
Communication loss	Watchdog 1 times out	$R_{FSMD} = 30\text{k}\Omega, 51\text{k}\Omega$ or $75\text{k}\Omega$ and no error-free communication	Enter fail-safe modes	CMWF1 bit	Pull low	Write CMWF1 bit to "0" or Exit fail-safe modes
Communication loss	Watchdog 2 times out	$R_{FSMD} = 30\text{k}\Omega, 51\text{k}\Omega$ or $75\text{k}\Omega$ and no error-free communication	Enter fail-safe modes	CMWF1 bit	Pull low	Write CMWF2 bit to "0" Feed the dog within the set WDT2 time range or Exit fail-safe modes
OTP data verification	OTP data ECC error	ECC2F_EN = 1	-	ECC_ST	Pull low	-

Note 8: OPENF, SHORTF, SLSHORTF, ISETSF, TSD, TF, LPBF, SCAVF, RSET_SH, EXF, CMWF1, RSET_OP, CMWF2 and CRCF bits are latched. Even though the fault conditions are removed, they cannot automatically reset to "0" but must be cleared by the host MCU writing it back to "0".

10.7 FUNCTIONAL SAFETY

The development of this product is based on a process according to ISO 26262 which has been certified to be compliant to ISO 26262 requirements and integrity levels up to ASIL D. Technical safety requirements for this product are rated ASIL B. In order to achieve the IC target metrics for the appropriate ASIL, it is mandatory to consider the safety mechanisms and recommendations mentioned in the safety manual.

10.7.1 TECHNICAL SAFETY REQUIREMENTS

Table 1.1-1: Technical Safety Requirements

TSR	Description of Technical Safety Requirements	ASIL
TSR1	The LED channel shall perform PWM duty cycle and output peak current according to a valid control or communication data (TSR1 is derived from FSR1)	ASIL B
TSR2	Status and diagnostics information shall be provided (TSR2 is derived from FSR2 and FSR3): • The IC shall provide function which allow to read back the actual state of the LED output channels • Diagnostic information shall be provided • Output channel cannot be controlled shall be detected and failure indication shall be provided • The IC will enter safe mode if it can't receive the host command	ASIL B

10.7.2 SAFE STATE

The Safe State for the IC depends on the particular rear bight function. Due to the fact that there is no allocation of IC channels to particular rear bight functions, it has to be considered that any rear bight function may be allocated to any channel of the IC. For that reason the IC implements a configurable fall-back concept for each channel, which allows the Safe State to adapt according to the requirements of the particular rear bight function.

10.7.3 FAULT TOLERANCE TIME TERRAIL

The diagnosis/safety mechanisms implemented in the IC have been specified in such a way that the Fault Detection and Reaction Times FFDt/FRT are compliant to the Fault Tolerant Time Interval requirements, which depend on the particular rear bight function. Due to the fact that there is no allocation of IC channels to particular rear bight functions, it has to be considered that any rear bight function may be allocated to any channel of the IC.

For that reason the most critical Fault Tolerant Time Interval requirement among all intended rear bight functions, which amounts to 300ms, has been considered.

10.8 UART INTERFACES

The host MCU can communicate with the IS32LT3138A device using a Universal Asynchronous Receiver and Transmitter (UART). The UART communication process uses a command and response protocol (LumiBus protocol) mastered by the host MCU to write and read the registers to and from each IS32LT3138A device. The IS32LT3138A UART interface utilizes half-duplex communications (transmit and receive cannot overlap). A tri-state buffer in the IS32LT3138A drives the TX out pin, so it is recommended to place an external pull-up resistor on the RX input return line of the host MCU. An external pull-up on the MCU TX output will allow multiple IS32LT3138A devices to share a common pair of TX and RX signals by connecting all IS32LT3138A TX lines together and all IS32LT3138A RX lines together. The baud rate can support 100kbps~1Mbps.

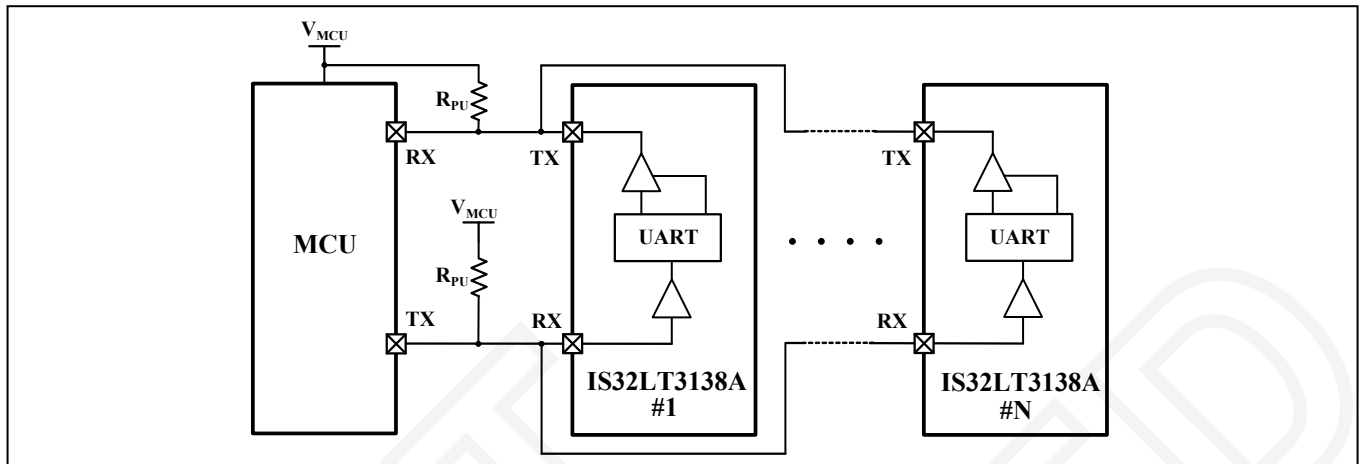


Figure 12 UART Interface Connection

Additionally, the physical TX and RX connections of IS32LT3138A can be joined together through a standard CAN transceiver (CAN PHY), as shown in Figure 13. This has the added advantage of protection from shorts to battery and/or shorts to ground on the cables and/or harnesses between the host MCU board and the IS32LT3138A board. The CAN physical layer has excellent EMI and EMS performance with long distance off-board connection.

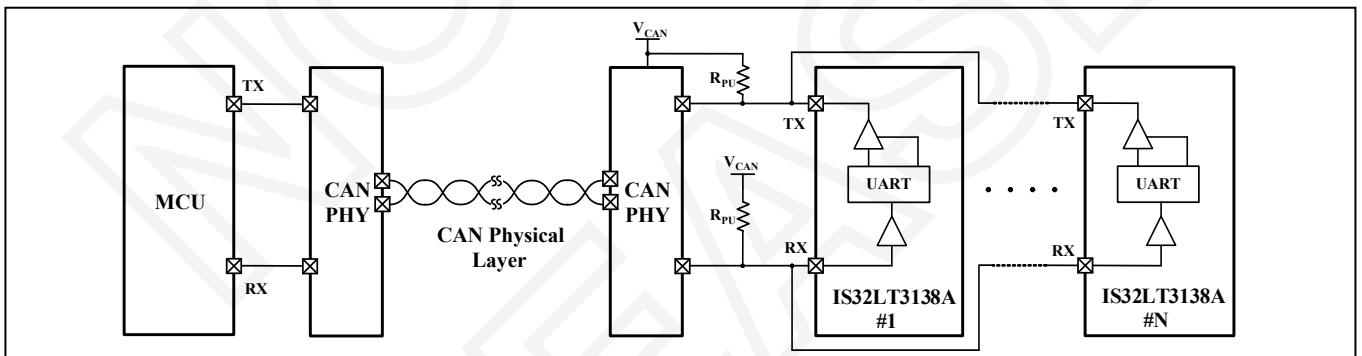


Figure 13 UART Interface with Standard CAN Transceiver Connection

10.8.1 UART DATA FORMAT

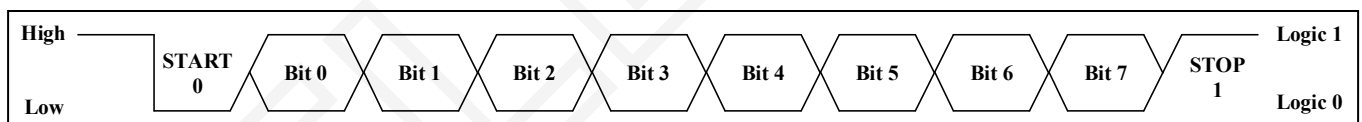


Figure 14 UART Data Byte Format

The UART operates with one start bit, eight data bits (LSbit first) and one stop bit. Above figure shows the waveform for an individual byte transfer on the UART. A logic "1" state occurs when the device drives the line to high voltage. A logic "0" state occurs when the device drives the line to ground. Below figure shows actual data bytes with UART data format.

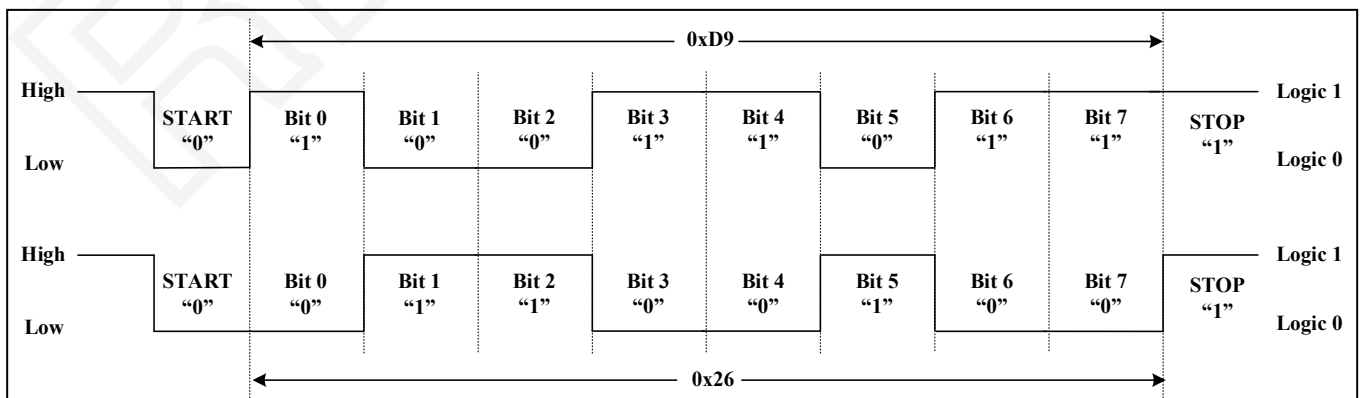


Figure 15 UART Data Transaction Example

The baud rate of UART communication can be 100kbps to 1Mbps which is synchronized by the baud rate of the SYNC byte of the BUS Reset command. The UART uses 32x over-sampling on the incoming asynchronous RX signal. Between UART data bytes, at least one bit is required as STOP bit.

10.8.2 LumiBus PROTOCOL

The communication uses the LumiBus protocol which is a UART-based protocol supported by most MCUs. The communication process of all three interfaces uses a command and response protocol mastered by the host MCU to write and read the registers to and from each IS32LT3138A device. This means that the IS32LT3138A device never initiates traffic onto the network. The LumiBus protocol maps the registers into an address space on each device. The host MCU uses the LumiBus protocol to initiate a communication transaction by sending a command frame. This command frame addresses either one IS32LT3138A device directly or broadcasts to all IS32LT3138A devices on the network. This addressing may cause a response frame to be sent back from the slave IS32LT3138A device depending on the command type of the command frame. There are four types of commands:

- 1) BUS Reset Command: resets the UART.
- 2) Write Command: writes data from host MCU to specific IS32LT3138A device(s).
- 3) Read Command: reads data from specific IS32LT3138A device to host MCU.
- 4) Special Command: specifies IS32LT3138A device(s) to implement specific function.

There is no response frame given following a broadcast write command frame. Therefore, only two types of response frames exist that an IS32LT3138A device sends back to the host MCU: Write Acknowledge (if enabled) and Read Response.

10.8.3 COMMAND FRAME TYPES

10.8.3.1 BUS Reset Command Frame

The host MCU can reset the device UART and LumiBus protocol state machine at any time by sending BUS Reset command. The BUS Reset command consists of reset signal and SYNC byte (0x55). The reset signal includes at 150 μ s~10ms break low and at 2 μ s~100 μ s logic high break delimiter. Upon receiving the bus reset signal, the LumiBus protocol state machine of all IS32LT3138A devices on the bus will be reset to a known-good state. The bus reset signal must be followed by a SYNC byte (0x55) send by desired baud rate (within 100kbps to 1Mbps) to synchronize the baud rate to all IS32LT3138A devices. The subsequent communication must use the identical baud rate. With this synchronization approach, the cost of an external crystal oscillator is saved. To avoid clock drifting over time and ambient temperature, it's recommended to periodically send a BUS Reset Command to the IS32LT3138A devices.

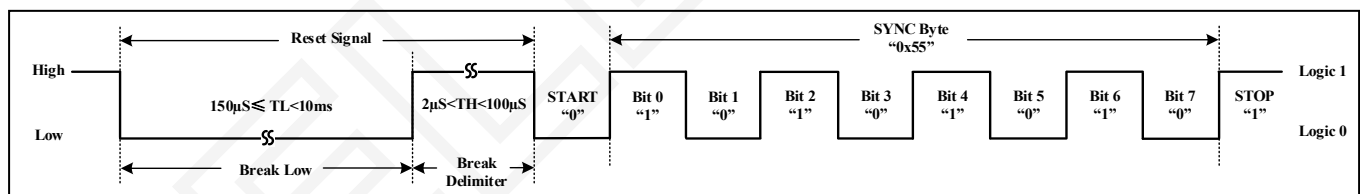


Figure 16 BUS Reset Command

Upon system power up, the host MCU must initialize the BUS by sending a BUS Reset Command before communication. This BUS reset operation can be optionally performed by the host MCU for several application scenarios: (1) upon system power up, (2) communication watchdog times out, (3) communication fault is detected, illustrated as in the following diagram:

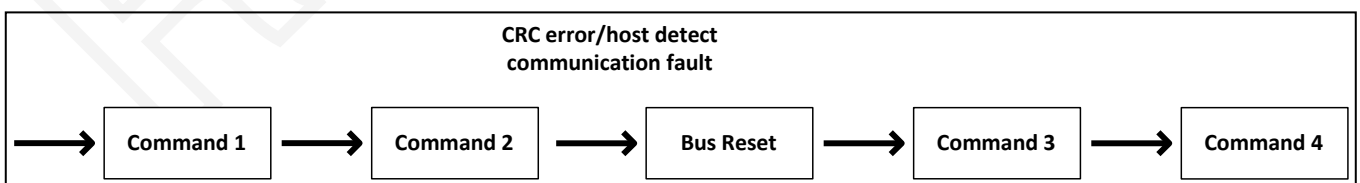


Figure 17 Communication Fault is Detected

Note that the BUS Reset command only resets the interface state machine (including stored communication baud rate). It does not reset the registers and does not halt normal LED PWM operation.

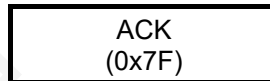
10.8.3.2 Write Command Frame

The Write Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	Data 1 (One Byte)	...	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)
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10.8.3.3 Acknowledge Frame

If the ACKEN bit is set in the SYSCFG register, the addressed device transmits an acknowledge back to the host MCU upon a successful single device write. The Acknowledge Frame is comprised of a single byte (ACK=0x7F) as the following sequence.



10.8.3.4 Read Command Frame (transferred by the host MCU)

The Read Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)
--------------------------------	-------------------------	--------------------------------------	---------------------	---------------------

A successfully-addressed IS32LT3138A device then transfers back the appropriate Read Response Frame.

The Read Response Frame is comprised of the following sequence.

RSP Frame Header (One Byte)	Device ID (One Byte)	Data 1 (One Byte)	...	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)
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10.8.3.5 Special Command Frame

The special command specifies the IS32LT3138A device to implement specific function which includes:

a) Update Command

This special command is used for below scenarios:

- Update the configuration of the PWM registers data and Scaling registers data into output stages at the next PWM boundary after this command is issued.
- Update the configuration of the DC_PWM_SEL register and PHASE_CTRL register (00h).

b) Registers Reset Command

Resets all registers to default value, excluding the PWR bit in SYSCFG register (4Ah).

The Special Command Frame is comprised of the following sequence:

CMD Frame Header (One Byte)	Device ID (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)
--------------------------------	-------------------------	---------------------	---------------------

One complete command frame can be received successfully even if the bytes in the frame is not sent continuously. CRC error could be determined by reading back the written data byte.



If host's watch dog time is disabled or time laps is within watchdog time

10.8.4 TRANSACTION FRAME DESCRIPTION

Command frames include the following byte types:

- 1) Frame Header Byte
- 2) Device ID Byte
- 3) Start Register Address Byte
- 4) N Data Byte(s) (N = 1~16, 32)

5) CRC Bytes (CRC_L and CRC_H)

6) Acknowledge Byte (ACK)

10.8.4.1 Frame Header Byte

The Frame Header Byte identifies the transaction as either a write/read command frame or a response frame. In addition, the Frame Header Byte indicates how many data bytes are being written/read or responded. The number of data bytes to be written/read or responded can be 1~16 or 32.

Frame Header Type	D7	D6	D5	D4	D3	D2	D1	D0
CMD Frame Header	FRM_TYPE	W/R	BCON	CMD				
RSP Frame Header	FRM_TYPE	RSVD	RSVD	RSP				

The fields shown in the Frame Header Byte above are described in the table below.

	Value (BIN)	Description
FRM_TYPE (Bit 7)	0	Response frame sent back from the IS32LT3138A device to host MCU
	1	Command frame sent from host MCU to the IS32LT3138A device
W/R (Bit 6)	0	Write command frame
	1	Read command frame
BCON (Bit 5)	0	Single device write or read.
	1	Broadcast write. The Device ID Byte must be 0xBF to broadcast to all IS32LT3138A devices. Broadcast only accepts write command
CMD (Bit 4:0)	Specify transmit data length for write/read command frame:	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length
	For special commands (W/R bit must be set to "0"):	
	11000	Update Command. Valid for both single device and broadcast write
	11110	Registers Reset Command. Valid for both single device and broadcast write
RSP (Bit 4:0)	Specify transmit data length for response frame:	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length

10.8.4.2 Device ID Byte

	D7	D6	D5	D4	D3	D2	D1	D0
Device ID	p[1]	p[0]	DEV_ID [5:0]					

There are six DEV_ID bits and two parity bits.

The parity bits for the Device ID byte are calculated with the equations below:

$$p[1] = \sim(\text{dev_id}[1] \wedge \text{dev_id}[3] \wedge \text{dev_id}[4] \wedge \text{dev_id}[5])$$

$$p[0] = \text{dev_id}[0] \wedge \text{dev_id}[1] \wedge \text{dev_id}[2] \wedge \text{dev_id}[4]$$

The device ID of each IS32LT3138A device is determined by the resistors connected from three address pins of ADDR0, ADDR1 and ADDR2 to GND. As following mapping for the Device ID byte. For a broadcast command of UART interface, the DEV_ID[5:0] must be 0b 111111, otherwise the broadcast command will be invalid.

R _{AD2}	R _{AD1}	R _{AD0}	D7	D6	D5	D4	D3	D2	D1	D0	DEVICE ID (HEX)
(kΩ, Note 9)											
10k	10k	10k	1	0	0	0	0	0	0	0	80
10k	10k	30k	0	1	0	1	0	0	0	0	50
10k	10k	51k	0	0	1	0	0	0	0	0	20
10k	10k	75k	1	1	1	1	0	0	0	0	F0
10k	30k	10k	1	1	0	0	0	1	0	0	C4
10k	30k	30k	0	0	0	1	0	1	0	0	14
10k	30k	51k	0	1	1	0	0	1	0	0	64
10k	30k	75k	1	0	1	1	0	1	0	0	B4
10k	51k	10k	0	0	0	0	1	0	0	0	08
10k	51k	30k	1	1	0	1	1	0	0	0	D8
10k	51k	51k	1	0	1	0	1	0	0	0	A8
10k	51k	75k	0	1	1	1	1	0	0	0	78
10k	75k	10k	0	1	0	0	1	1	0	0	4C
10k	75k	30k	1	0	0	1	1	1	0	0	9C
10k	75k	51k	1	1	1	0	1	1	0	0	EC
10k	75k	75k	0	0	1	1	1	1	0	0	3C
30k	10k	10k	1	1	0	0	0	0	0	1	C1
30k	10k	30k	0	0	0	1	0	0	0	1	11
30k	10k	51k	0	1	1	0	0	0	0	1	61
30k	10k	75k	1	0	1	1	0	0	0	1	B1
30k	30k	10k	1	0	0	0	0	1	0	1	85
30k	30k	30k	0	1	0	1	0	1	0	1	55
30k	30k	51k	0	0	1	0	0	1	0	1	25
30k	30k	75k	1	1	1	1	0	1	0	1	F5
30k	51k	10k	0	1	0	0	1	0	0	1	49
30k	51k	30k	1	0	0	1	1	0	0	1	99
30k	51k	51k	1	1	1	0	1	0	0	1	E9
30k	51k	75k	0	0	1	1	1	0	0	1	39
30k	75k	10k	0	0	0	0	1	1	0	1	0D
30k	75k	30k	1	1	0	1	1	1	0	1	DD
30k	75k	51k	1	0	1	0	1	1	0	1	AD
30k	75k	75k	0	1	1	1	1	1	0	1	7D
51k	10k	10k	0	1	0	0	0	0	1	0	42
51k	10k	30k	1	0	0	1	0	0	1	0	92
51k	10k	51k	1	1	1	0	0	0	1	0	E2
51k	10k	75k	0	0	1	1	0	0	1	0	32
51k	30k	10k	0	0	0	0	0	1	1	0	06
51k	30k	30k	1	1	0	1	0	1	1	0	D6
51k	30k	51k	1	0	1	0	0	1	1	0	A6
51k	30k	75k	0	1	1	1	0	1	1	0	76
51k	51k	10k	1	1	0	0	1	0	1	0	CA
51k	51k	30k	0	0	0	1	1	0	1	0	1A
51k	51k	51k	0	1	1	0	1	0	1	0	6A
51k	51k	75k	1	0	1	1	1	0	1	0	BA

51k	75k	10k	1	0	0	0	1	1	1	0	8E
51k	75k	30k	0	1	0	1	1	1	1	0	5E
51k	75k	51k	0	0	1	0	1	1	1	0	2E
51k	75k	75k	1	1	1	1	1	1	1	0	FE
75k	10k	10k	0	0	0	0	0	0	1	1	03
75k	10k	30k	1	1	0	1	0	0	1	1	D3
75k	10k	51k	1	0	1	0	0	0	1	1	A3
75k	10k	75k	0	1	1	1	0	0	1	1	73
75k	30k	10k	0	1	0	0	0	1	1	1	47
75k	30k	30k	1	0	0	1	0	1	1	1	97
75k	30k	51k	1	1	1	0	0	1	1	1	E7
75k	30k	75k	0	0	1	1	0	1	1	1	37
75k	51k	10k	1	0	0	0	1	0	1	1	8B
75k	51k	30k	0	1	0	1	1	0	1	1	5B
75k	51k	51k	0	0	1	0	1	0	1	1	2B
75k	51k	75k	1	1	1	1	1	0	1	1	FB
75k	75k	10k	1	1	0	0	1	1	1	1	CF
75k	75k	30k	0	0	0	1	1	1	1	1	1F
75k	75k	51k	0	1	1	0	1	1	1	1	6F
75k	75k	75k	1	0	1	1	1	1	1	1	BF
-	-	-	1	0	1	1	1	1	1	1	BF(Note 10) (for broadcast command only)

Note 9: The tolerance range of resistance accuracy could be $\pm 1\%$ for 10k, 30k, 51K and 75k.

Note 10: The Device ID Byte must be 0xBF to broadcast to all IS32LT3138A devices. Broadcast only accepts write command.

10.8.4.3 Start Register Address Byte

The LumiBus protocol allows up to 32 successive register locations from the addressed register to be written or read by a single command frame. The Start Register Address Byte is single byte which specifies the first register being written or read. The Start Register Address byte is present in only Write and Read Command transactions, not in Read Response and Special command transactions.

10.8.4.4 N Data Byte (s)

The Frame Header Byte specifies the number of data bytes to be included in the frame.

10.8.4.5 CRC Bytes (CRC_L and CRC_H)

The host MCU sends command to IS32LT3138A using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame bytes, e.g., Frame Header Byte, Device ID Byte, Start Register Address Byte, N Data Bytes. Lower byte first followed by higher byte. The CRC Bytes allow detection of errors within the transaction frame. The device increments the CRC Error Count Register (52h) each time a CRC error occurs on an incoming command frame and the CRCF bit in FLT_TYPE_1 register (50h) will be set to "1" and the FAULTB pin will go low to report fault condition after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRCF bit in FLT_TYPE_1 register (50h) is latched, which means that it cannot automatically reset to "0" when no CRC error occurs but must be cleared by the host MCU writing it back to "0". Once the CRCF bit is cleared, the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRC bytes are also calculated by the addressed device during its Read Response. The CRC bytes are then appended to the end of the read data, lower byte first followed by higher byte. This allows the host MCU to check the read data coming from the IS32LT3138A device for any transmission errors. The following is a reference CRC checksum C code for a transmission to the IS32LT3138A devices.

```

1. Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
2. {
3.     Uint16 crc = 0;
4.     Uint16 I;
5.     while (len--)
6.     {
7.         crc ^= *buf++;
8.         for (I = 0; I < 8; I++)
9.         {
10.            crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
11.        }
12.    }
13.    return crc;
14. }
15.

```

Upon reading data from the IS32LT3138A device, the host MCU should calculate and compare the CRC to determine whether valid data was received. When IS32LT3138A sends back CRC bytes to the host MCU, the calculated CRC bytes must be bit-reversed before comparison to the received CRC bytes. The following is a reference code to perform received CRC bit reversal.

```

1. Uint8 reverse_byte(Uint8 byte)
2. {
3.     // First, swap the nibbles
4.     byte = (((byte & 0xF0) >> 4) | ((byte & 0x0F) << 4));
5.     // Then, swap bit pairs
6.     byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
7.     // Finally, swap adjacent bits
8.     byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
9.     // We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
10.    return byte;
11. }
12.

```

The following is a reference code for checking the read data against received CRC bytes.

```

1. bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
2. {
3.     Uint16 crc_calc; // Calculated CRC
4.     Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
5.     // Calculate the CRC based on bytes received
6.     crc_calc = crc_16_ibm(rx_buf, crc_start);
7.     crc_lsb = (crc_calc & 0x00FF);
8.     crc_msb = ((crc_calc >> 8) & 0x00FF);
9.     // Perform the bit reversal within each byte
10.    crc_msb = reverse_byte(crc_msb);
11.    crc_lsb = reverse_byte(crc_lsb);
12.    // Do they match?
13.    if((* (rx_buf + crc_start) == crc_lsb) && (* (rx_buf + crc_start + 1) == crc_msb))
14.    {
15.        return TRUE;
16.    }
17.    else
18.    {
19.        return FALSE;
20.    }
21. }
22.

```

10.8.4.6 Acknowledge Byte

The Acknowledge Byte ("ACK") consists of a single byte (ACK=0x7F):

ACK is sent back by the addressed IS32LT3138A device only if the ACKEN bit is set in the SYSCFG register (42h) and only if the write is successful. A successful write yields no CRC checksum error or parity errors. Note that the acknowledge is only valid for single device write transaction of IS32LT3138A.

10.8.4.7 Turnaround Time

When considering back-to-back data transfer, the turnaround time (additional time required between the end of the previous byte stop bit and the beginning of the next byte start bit) is required, that means a finite amount of dead time must be inserted between two bytes or two command frames. It's recommended to use dual stop bits mode for the UART interface.

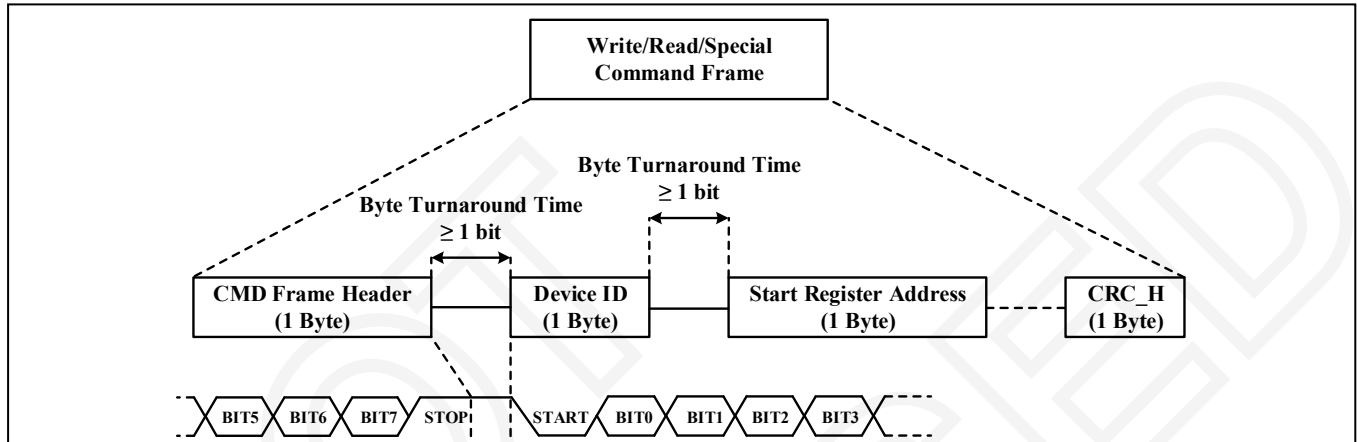


Figure 18 Turnaround Time Between Byte to Byte

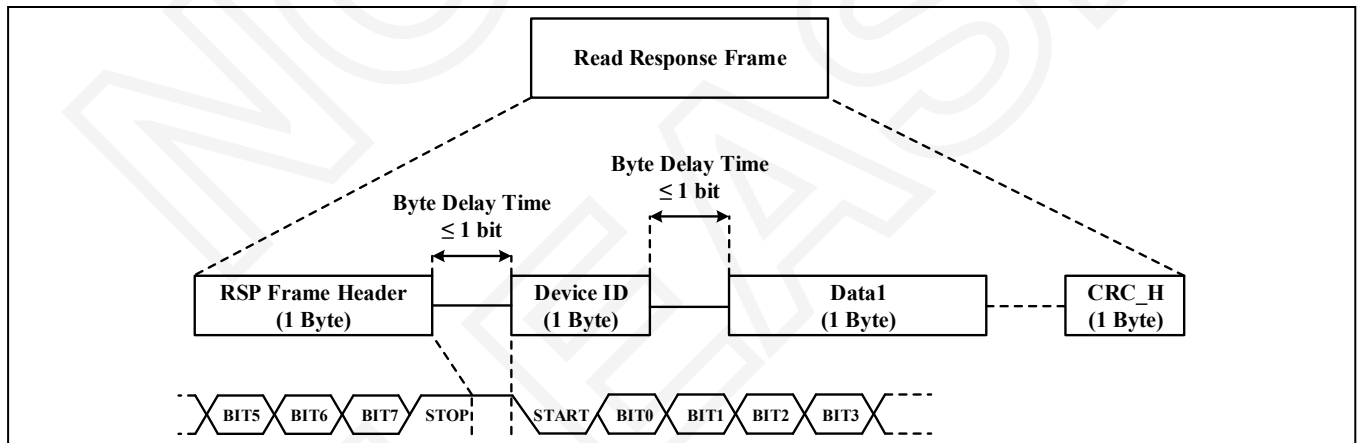


Figure 19 Delay Time Between Byte to Byte of Read Response Frame

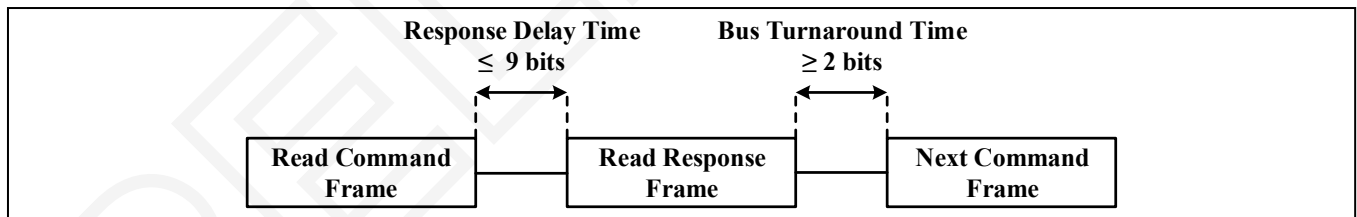


Figure 20 Turnaround Time Between Read Response Frame to Next Command Frame

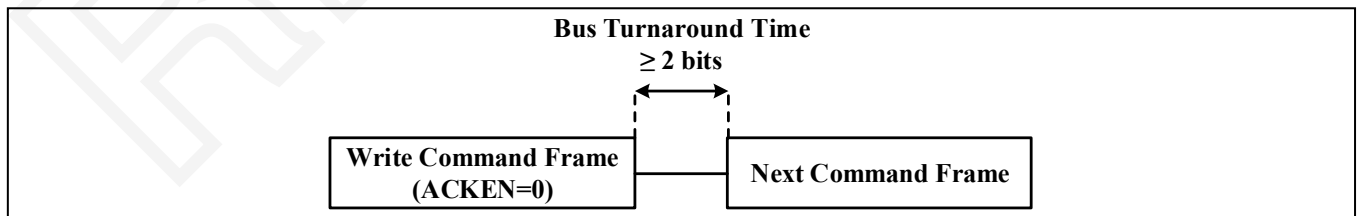


Figure 21 Turnaround Time Between Write Command Frame to Next Command Frame (ACK Disabled)

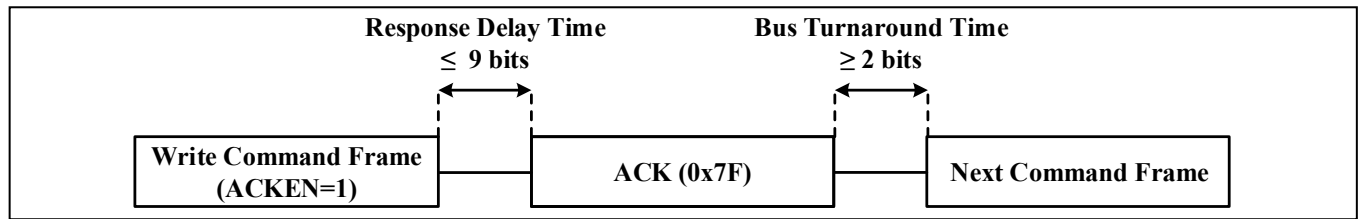


Figure 22 Turnaround Time Between ACK to Next Command Frame (ACK Enabled)

10.9 COMMUNICATIONS EXAMPLES

The total number of transmitted bytes depends on the specific task being performed. The examples below show the sequence of transmitted bytes for a given transaction.

10.9.1 EXAMPLE 1: SINGLE DEVICE WRITE OF 3 BYTES

Write to Device ID with parity = 0x55, $R_{AD0}=30k\Omega$, $R_{AD1}=30k\Omega$, $R_{AD2}=30k\Omega$: beginning at register 26h, PWM1_H=0x1F, PWM2_H=0x2F, PWM1_2_L=0x3F.

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

Interface	Command Frame							
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART	0x82 (0b10000010)	0x55	0x26	0x1F	0x2F	0x3F	0x74	0x80

Acknowledge from addressed device (if enabled ACKEN bit for IS32LT3138A)

Acknowledge Frame	
ACK	
0x7F	

10.9.2 EXAMPLE 2: SINGLE DEVICE READ OF 2 BYTES

Read from Device ID with parity = 0xA3, $R_{AD0}=51k\Omega$, $R_{AD1}=10k\Omega$, $R_{AD2}=75k\Omega$: beginning at register 57H, read FLT_TYPE

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
CRC Bytes	2
Total	5

	Command Frame				
Interface	CMD Frame Header	Device ID	Start Register Address	CRC_L	CRC_H
UART	0xC1 (0b11000001)	0xA3	0x57	0x68	0xF2

Read Response: FLT_TYPE=0x00

Byte Types	Number of Bytes
RSP Frame Header Byte	1
Device ID Byte	1
Data Bytes	2
CRC Bytes	2
Total	6

	Command Frame					
Interface	RSP Frame Header	Device ID	Data 1	Data 2	CRC_L	CRC_H
UART	0x01 (0b00000001)	0xA3	0x00	0x00	0x8F	0x7B

10.9.3 EXAMPLE 3: BROADCAST WRITE OF 3 BYTES

Broadcast write to all devices (fixed Device ID with parity = 0xBF): beginning at register 14h, SCA1=0x0F, SCA2=0x1F, SCA3=0x2F.

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

	Command Frame							
Interface	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART	0xA2 (0b10100010)	0xBF	0x14	0x0F	0x1F	0x2F	0x70	0x86

10.9.4 EXAMPLE 4: BROADCAST REGISTERS RESET COMMAND (SPECIAL COMMAND)

Broadcast Registers Reset Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	CMD Frame Header	Device ID	CRC_L	CRC_H
UART	0xBE (0b10111110)	0xBF	0x30	0x10

10.9.5 EXAMPLE 5: BROADCAST UPDATE COMMAND (SPECIAL COMMAND)

Broadcast Update Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	CMD Frame Header	Device ID	CRC_L	CRC_H
UART	0xB8 (0b10111000)	0xBF	0x33	0xB0

10.10 DEVICE FUNCTIONAL MODES

The IS32LT3138A device operates in one of several states.

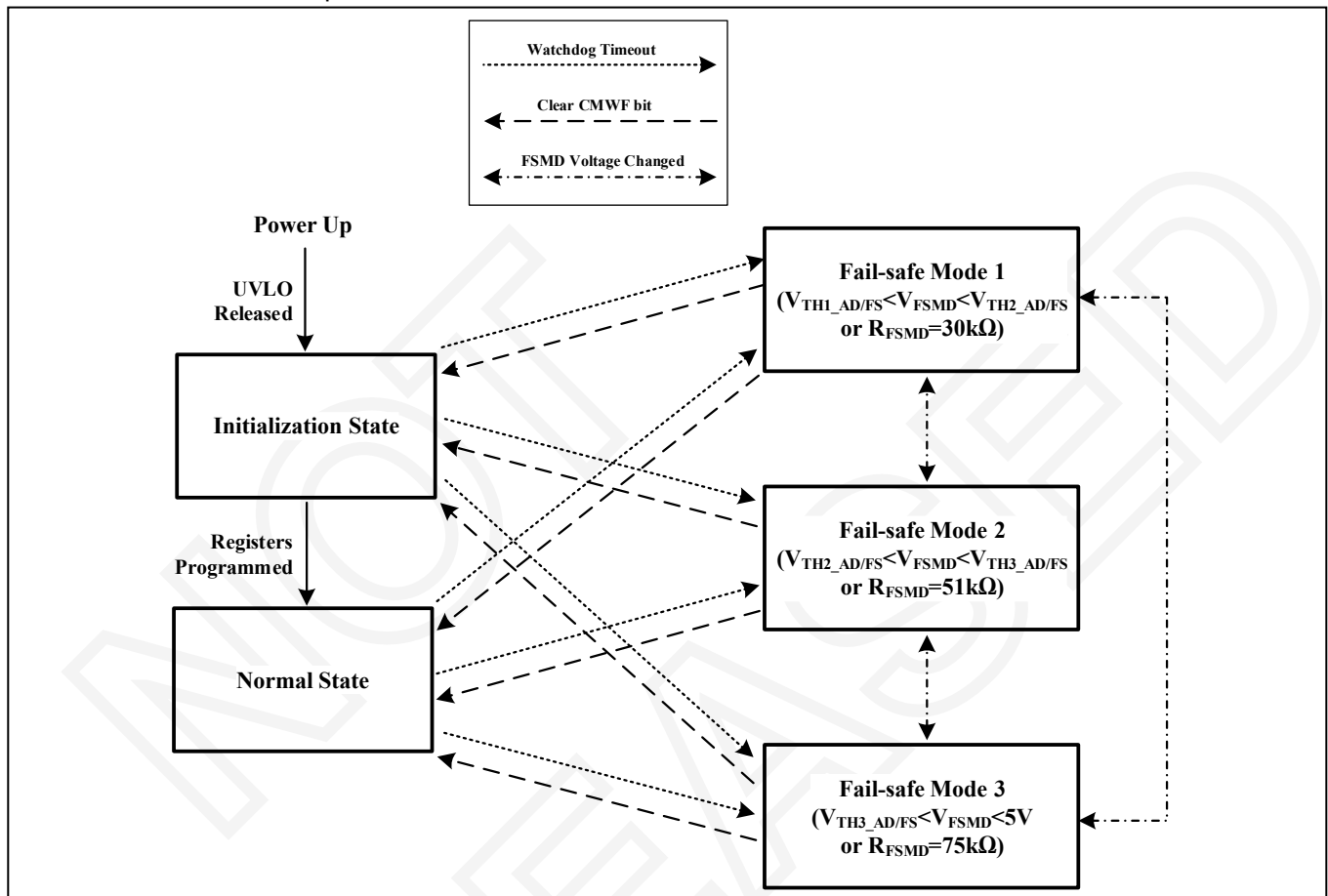


Figure 23 Operation States

10.10.1 INITIALIZATION STATE

On power up and once released from UVLO, the device enters an initialization state. In this state, all registers are reset to default values and all outputs are in off state. The device waits to receive commands from the MCU master.

10.10.2 NORMAL STATE

In normal state, the IS32LT3138A registers control its outputs by accepting interface commands and by monitoring and responding to realtime events on the inputs associated with the analog and power circuitry. This allows dimming of the LED output using the registers settings.

10.10.3 FAIL-SAFE STATE

This state allows the user to preset the outputs' state if the communication is broken. The device integrates a communication watchdog timer that operates based on the system clock pulse. IS32LT3138A has two internal watchdog timers, watchdog timer 1 is a communication watchdog timer, programmed through the CMWT1 register (82h), defining the time of the communication watchdog timer. The watchdog timer 2 is the command watchdog timer, programmed through the CMWT2 register (83h), which defines the maximum/minimum feeding time range of the command watchdog timer. If the communication watchdog times out (no error-free communication is successfully received within the set number of system clock cycles) or the command watchdog overflows (no feeding command is successfully received within the set time range of feeding dog), the device will enter the fail-proof mode, including three modes: Mode 1 ~ Mode 3.

The FSMD pin is used to configure the fail-safe modes. When the resistor R_{FSMD} is connected from the FSMD pin to ground, the internal $I_{AD/FS}$ (typical 50 μ A) current source creates a voltage on the FSMD pin, V_{FSMD} . The device compares the V_{FSMD} with internal different reference voltage levels ($V_{TH1_AD/FS}$, $V_{TH2_AD/FS}$ and $V_{TH3_AD/FS}$) to determine the fail-safe mode. It also allows to externally apply proper voltage on the FSMD pin to either choose or change the fail-safe mode. Refer to the Fail-safe Mode Setting Table.

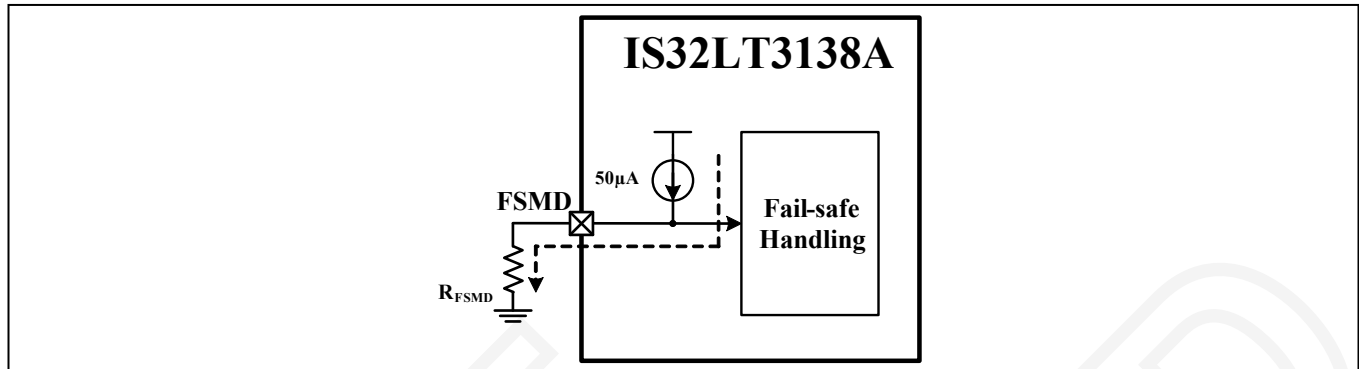


Figure 24 Fail-safe Mode Setting

When $0V < V_{FSMD} < V_{TH1_AD/FS}$, or $R_{FSMD} = 10k\Omega$, the internal communication watchdog is invalid, and the fail-safe mode is disabled. The outputs are always controlled by the scaling and PWM registers (03h~14h).

When $V_{TH1_AD/FS} < V_{FSMD} < V_{TH2_AD/FS}$, or $R_{FSMD} = 30k\Omega$, the internal communication watchdog 1 and Command watchdog 2 is active, and the fail-safe mode is Mode 1. If the watchdog times out, the device will enter fail-safe Mode 1 and the outputs will be determined by the OTP-A DEFAULT registers (B1h~BEh). The CMWF 2 or CMW F1 bit in FLT_TYPE_1 register (50h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FLT_TYPE_1 register (50h) must be cleared by the host MCU writing it to "0", and feed the watchdog 2 for the set time. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH2_AD/FS} < V_{FSMD} < V_{TH3_AD/FS}$, or $R_{FSMD} = 51k\Omega$, the internal communication watchdog 1 and Command watchdog 2 is active, and the fail-safe mode is Mode 2. If the watchdog times out, the device will enter fail-safe Mode 2 and all outputs will be forced into completely off. The CMWF 2 or CMW F1 bit in FLT_TYPE_1 register (50h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FLT_TYPE_1 register (50h) must be cleared by the host MCU writing it to "0" and feed the watchdog 2 for the set time. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH3_AD/FS} < V_{FSMD} < 5V$, or $R_{FSMD} = 75k\Omega$, the internal communication watchdog 1 and Command watchdog 2 is active, and the fail-safe mode is Mode 3. If the watchdog times out, the device will enter fail-safe Mode 3 and all outputs will be forced into fully on (with Max PWM duty cycle). The CMWF 2 or CMW F1 bit in FLT_TYPE_1 register (50h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FLT_TYPE_1 register (50h) must be cleared by the host MCU writing it to "0" and feed the watchdog 2 for the set time. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

In the fail-safe modes, the fault protections also are valid, including LED string open/short, single LED short, overcurrent (ISET shorted), and over temperature. It should be noted that even if OUT16~OUT18 is set to the Special function through this register, after entering the Fail-safe mode, the Special Function pin will be set to LED OUT, and the Special Function will fail. When using DCFB function, special care should be taken not to use Fail-safe Mode 3 Mode, and the DEFLED 16 bit of DEFLED3 register (B5h) should be set to LED off when using Fail-safe Mode 1. To avoid the DCFB pin pulling current causing a catastrophic failure of the DCDC.

Note that the device must be re-initialized after quitting from the fail-safe mode to normal state.

10.10.4 FAIL-SAFE MODE SETTING TABLE

FSMD Pin	Fail-Safe Mode	LED State in Fail-Safe Mode
$0V < V_{FSMD} < V_{TH1_AD/FS}$ or $R_{FSMD} = 10k\Omega$	Disabled	-
$V_{TH1_AD/FS} < V_{FSMD} < V_{TH2_AD/FS}$ or $R_{FSMD} = 30k\Omega$	Mode 1	Determined by OTP (B0h~BEh)
$V_{TH2_AD/FS} < V_{FSMD} < V_{TH3_AD/FS}$ or $R_{FSMD} = 51k\Omega$	Mode 2	All Completely Off
$V_{TH3_AD/FS} < V_{FSMD} < 5V$ or $R_{FSMD} = 68k\Omega$	Mode 3	All On with Max PWM duty cycle

11 REGISTER MAP

11.1 REGISTER MAP

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT	
00	CONFIG	-	PFS[2:0]			OFA[1:0]		PDE	DC_PWM	R/W	0b 00111110	
01	GC_CTRL	-	-	GCC [5:0]							R/W	0b 00111111
02	TEMP_SEN	-	-	-	-	-	TROF [2:0]			R/W	0b 00000000	
03	SCA1	-	SCA1_DATA [6:0]							R/W	0b 01111111	
04	SCA2	-	SCA2_DATA [6:0]							R/W	0b 01111111	
05	SCA3	-	SCA3_DATA [6:0]							R/W	0b 01111111	
06	SCA4	-	SCA4_DATA [6:0]							R/W	0b 01111111	
07	SCA5	-	SCA5_DATA [6:0]							R/W	0b 01111111	
08	SCA6	-	SCA6_DATA [6:0]							R/W	0b 01111111	
09	SCA7	-	SCA7_DATA [6:0]							R/W	0b 01111111	
0A	SCA8	-	SCA8_DATA [6:0]							R/W	0b 01111111	
0B	SCA9	-	SCA9_DATA [6:0]							R/W	0b 01111111	
0C	SCA10	-	SCA10_DATA [6:0]							R/W	0b 01111111	
0D	SCA11	-	SCA11_DATA [6:0]							R/W	0b 01111111	
0E	SCA12	-	SCA12_DATA [6:0]							R/W	0b 01111111	
0F	SCA13	-	SCA13_DATA [6:0]							R/W	0b 01111111	
10	SCA14	-	SCA14_DATA [6:0]							R/W	0b 01111111	
11	SCA15	-	SCA15_DATA [6:0]							R/W	0b 01111111	
12	SCA16	-	SCA16_DATA [6:0]							R/W	0b 01111111	
13	SCA17	-	SCA17_DATA [6:0]							R/W	0b 01111111	
14	SCA18	-	SCA18_DATA [6:0]							R/W	0b 01111111	
15	PWM1_H	PWM1_DATA [15:8]							R/W	0b 00000000		
16	PWM1_L	PWM1_DATA [7:0]							R/W	0b 00000000		
17	PWM2_H	PWM2_DATA [15:8]							R/W	0b 00000000		
18	PWM2_L	PWM2_DATA [7:0]							R/W	0b 00000000		
19	PWM3_H	PWM3_DATA [15:8]							R/W	0b 00000000		
1A	PWM3_L	PWM3_DATA [7:0]							R/W	0b 00000000		
1B	PWM4_H	PWM4_DATA [15:8]							R/W	0b 00000000		
1C	PWM4_L	PWM4_DATA [7:0]							R/W	0b 00000000		
1D	PWM5_H	PWM5_DATA [15:8]							R/W	0b 00000000		
1E	PWM5_L	PWM5_DATA [7:0]							R/W	0b 00000000		
1F	PWM6_H	PWM6_DATA [15:8]							R/W	0b 00000000		
20	PWM6_L	PWM6_DATA [7:0]							R/W	0b 00000000		
21	PWM7_H	PWM7_DATA [15:8]							R/W	0b 00000000		
22	PWM7_L	PWM7_DATA [7:0]							R/W	0b 00000000		
23	PWM8_H	PWM8_DATA [15:8]							R/W	0b 00000000		
24	PWM8_L	PWM8_DATA [7:0]							R/W	0b 00000000		
25	PWM9_H	PWM9_DATA [15:8]							R/W	0b 00000000		
26	PWM9_L	PWM9_DATA [7:0]							R/W	0b 00000000		
27	PWM10_H	PWM10_DATA [15:8]							R/W	0b 00000000		
28	PWM10_L	PWM10_DATA [7:0]							R/W	0b 00000000		
29	PWM11_H	PWM11_DATA [15:8]							R/W	0b 00000000		
2A	PWM11_L	PWM11_DATA [7:0]							R/W	0b 00000000		
2B	PWM12_H	PWM12_DATA [15:8]							R/W	0b 00000000		
2C	PWM12_L	PWM12_DATA [7:0]							R/W	0b 00000000		

2D	PWM13_H	PWM13_DATA [15:8]								R/W	0b 00000000
2E	PWM13_L	PWM13_DATA [7:0]								R/W	0b 00000000
2F	PWM14_H	PWM14_DATA [15:8]								R/W	0b 00000000
30	PWM14_L	PWM14_DATA [7:0]								R/W	0b 00000000
31	PWM15_H	PWM15_DATA [15:8]								R/W	0b 00000000
32	PWM15_L	PWM15_DATA [7:0]								R/W	0b 00000000
33	PWM16_H	PWM16_DATA [15:8]								R/W	0b 00000000
34	PWM16_L	PWM16_DATA [7:0]								R/W	0b 00000000
35	PWM17_H	PWM17_DATA [15:8]								R/W	0b 00000000
36	PWM17_L	PWM17_DATA [7:0]								R/W	0b 00000000
37	PWM18_H	PWM18_DATA [15:8]								R/W	0b 00000000
38	PWM18_L	PWM18_DATA [7:0]								R/W	0b 00000000
39	LED1_2_SLS	LED2_SLSTH[3:0]				LED1_SLSTH [3:0]				R/W	0b 00000000
3A	LED3_4_SLS	LED4_SLSTH[3:0]				LED3_SLSTH [3:0]				R/W	0b 00000000
3B	LED5_6_SLS	LED6_SLSTH[3:0]				LED5_SLSTH [3:0]				R/W	0b 00000000
3C	LED7_8_SLS	LED8_SLSTH[3:0]				LED7_SLSTH [3:0]				R/W	0b 00000000
3D	LED9_10_SLS	LED10_SLSTH[3:0]				LED9_SLSTH [3:0]				R/W	0b 00000000
3E	LED11_12_SLS	LED12_SLSTH[3:0]				LED11_SLSTH [3:0]				R/W	0b 00000000
3F	LED13_14_SLS	LED14_SLSTH[3:0]				LED13_SLSTH [3:0]				R/W	0b 00000000
40	LED15_16_SLS	LED16_SLSTH[3:0]				LED15_SLSTH [3:0]				R/W	0b 00000000
41	LED17_18_SLS	LED18_SLSTH[3:0]				LED17_SLSTH [3:0]				R/W	0b 00000000
42	SYSCFG	SSCEN	SSC [1:0]		ACKEN	-	-	-	PWR	R/W	0b 00000000
43	FS_FLTL	-	SHORT_FLT[2:0]			FLT_UV[3:0]				R/W	0b 00000100
44	FLT_DET_EN	-	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	R/W	0b 00001111
45	FLT_CONFIG	-	SHCR	OPENC_R	SLSHCR	FT[3:0]				R/W	0b 01100011
46	SHORT_FLT1	-	-	SHORT_FLT[6:1]						R	0b 00000000
47	SHORT_FLT2	-	-	SHORT_FLT[12:7]						R	0b 00000000
48	SHORT_FLT3	-	-	SHORT_FLT[18:13]						R	0b 00000000
49	OPEN_FLT1	-	-	OPEN_FLT[6:1]						R	0b 00000000
4A	OPEN_FLT2	-	-	OPEN_FLT[12:7]						R	0b 00000000
4B	OPEN_FLT3	-	-	OPEN_FLT[18:13]						R	0b 00000000
4C	SLS_FLT1	-	-	SLS_FLT[6:1]						R	0b 00000000
4D	SLS_FLT2	-	-	SLS_FLT[12:7]						R	0b 00000000
4E	SLS_FLT3	-	-	SLS_FLT[18:13]						R	0b 00000000
4F	FAULT_EN	ECC2F_EN	SCAF_EN	DUTYF_EN	TFE	CRCFE	RSET_OPE	RSET_SH_E	TSDE	R/W	0b 11111111
50	FAULT_TYPE_1	-	CMWF2	CMWF1	TF	CRCF	RSET_OP	RSET_SH	TSD	R/W	0b 00000000
51	FAULT_TYPE_2	SCAVF	LPBF	-	-	EXF	SLSHORTF	SHORTF	OPENF	R/W	0b 00000000
52	CERRCNT	CERRCNT [7:0]								R/W	0b 00000000
53	CH_FS	OUT18_FS	OUT17_FS	OUT16_FS	OUTADC_N	-	-	DCFB_N[1:0]		R/W	0b 00000000
54	DCFB_OCS	DCFB_OUT[7:0]								R/W	0b 10000000
55	CHSEL_1	CHSEL[7:0]								R/W	0b 00000000
56	CHSEL_2	CHSEL[15:8]								R/W	0b 00000000
57	CHSEL_3	CHSEL[23:16]								R/W	0b 00000000
58	CHSEL_4	-	-	-	-	-	-	CHSEL[25:24]		R/W	0b 00000000
59	ADCCFG	OUT18_FCH[3:0]				OUT_SE_L	ADCSH[1:0]		ADCEN	R/W	0b 00000000
5A	ADCCTL	ADCCY_C_F	-	-	ADCRST	-		LOOP	SADC	R/W	0b 00000010

5B	ADC_OUT1_H	ADC_OUT1[9:2]						R	0b 00000000	
5C	ADC_OUT2_H	ADC_OUT2[9:2]						R	0b 00000000	
5D	ADC_OUT3_H	ADC_OUT3[9:2]						R	0b 00000000	
5E	ADC_OUT4_H	ADC_OUT4[9:2]						R	0b 00000000	
5F	ADC_OUT1_2_3_4_L	ADC_OUT4[1:0]	ADC_OUT3[1:0]	ADC_OUT2[1:0]		ADC_OUT1[1:0]		R	0b 00000000	
60	ADC_OUT5_H	ADC_OUT5[9:2]						R	0b 00000000	
61	ADC_OUT6_H	ADC_OUT6[9:2]						R	0b 00000000	
62	ADC_OUT7_H	ADC_OUT7[9:2]						R	0b 00000000	
63	ADC_OUT8_H	ADC_OUT8[9:2]						R	0b 00000000	
64	ADC_OUT5_6_7_8_L	ADC_OUT8[1:0]	ADC_OUT7[1:0]	ADC_OUT6[1:0]		ADC_OUT5[1:0]		R	0b 00000000	
65	ADC_OUT9_H	ADC_OUT9[9:2]						R	0b 00000000	
66	ADC_OUT10_H	ADC_OUT10[9:2]						R	0b 00000000	
67	ADC_OUT11_H	ADC_OUT11[9:2]						R	0b 00000000	
68	ADC_OUT12_H	ADC_OUT12[9:2]						R	0b 00000000	
69	ADC_OUT9_10_11_12_L	ADC_OUT12[1:0]	ADC_OUT11[1:0]	ADC_OUT10[1:0]		ADC_OUT9[1:0]		R	0b 00000000	
6A	ADC_OUT13_H	ADC_OUT13[9:2]						R	0b 00000000	
6B	ADC_OUT14_H	ADC_OUT14[9:2]						R	0b 00000000	
6C	ADC_OUT15_H	ADC_OUT15[9:2]						R	0b 00000000	
6D	ADC_OUT16_H	ADC_OUT16[9:2]						R	0b 00000000	
6E	ADC_OUT13_14_15_16_L	ADC_OUT16[1:0]	ADC_OUT15[1:0]	ADC_OUT14[1:0]		ADC_OUT13[1:0]		R	0b 00000000	
6F	ADC_OUT17_H	ADC_OUT17[9:2]						R	0b 00000000	
70	ADC_OUT18_H	ADC_OUT18[9:2]						R	0b 00000000	
71	ADC_OUT17_18_L	-	-	-	-	ADC_OUT18[1:0]	ADC_OUT17[1:0]	R	0b 00000000	
72	ADC_VREF_H	ADC_VREF [9:2]						R	0b 00000000	
73	ADC_VREF_L	-	-	-	-	-	ADC_VREF [1:0]	R	0b 00000000	
74	ADC_VPTAT_H	ADC_VPTAT [9:2]						R	0b 00000000	
75	ADC_VPTAT_L	-	-	-	-	-	ADC_VPTAT [1:0]	R	0b 00000000	
76	ADC_VDD_H	ADC_VDD [9:2]						R	0b 00000000	
77	ADC_VDD_L	-	-	-	-	-	ADC_VDD [1:0]	R	0b 00000000	
78	ADC_VIN_H	ADC_VIN [9:2]						R	0b 00000000	
79	ADC_VIN_L	-	-	-	-	-	ADC_VIN [1:0]	R	0b 00000000	
7A	ADC_VADJ_H	ADC_VADJ [9:2]						R	0b 00000000	
7B	ADC_VADJ_L	-	-	-	-	-	ADC_VADJ [1:0]	R	0b 00000000	
7C	ADC_VBG_H	ADC_VBG [9:2]						R	0b 00000000	
7D	ADC_VBG_L	-	-	-	-	-	ADC_VBG [1:0]	R	0b 00000000	
7E	ADC_IN1_H	ADC_IN1 [9:2]						R	0b 00000000	
7F	ADC_IN1_L	-	-	-	-	-	ADC_IN1 [1:0]	R	0b 00000000	
80	ADC_IN2_H	ADC_IN2 [9:2]						R	0b 00000000	
81	ADC_IN2_L	-	-	-	-	-	ADC_IN2 [1:0]	R	0b 00000000	
82	CMWT1	-	-	-	-	CMWTAP [2:0]		R/W	0b 00000011	
83	CMWT2	-	TDT2CLR	WDT2_MAX[2:0]		WDT2_MIN[2:0]		R/W	0b 00011000	
verification										
90	BSTSTA	-	-	-	-	-	FAIL	FINISH	R/W	0b 00000000
91	VFYCTL	MODE[1:0]		-	TOLERANCE[4:0]			R/W	0b 00000001	
92	VFYCFG	START/BUSY	-	-	VFYCHSEL[4:0]			R/W	0b 00000000	

93	DUTYF_1	DUTYFLT[8:1]							R	0b 00000000	
94	DUTYF_2	DUTYFLT[16:9]							R	0b 00000000	
95	DUTYF_3	-	-	-	-	-	-	DUTYFLT[18:17]	R	0b 00000000	
96	PWMDUTY_H	PWMDUTY[15:8]							R	0b 00000000	
97	PWMDUTY_L	PWMDUTY[7:0]							R	0b 00000000	
98	SEL_PWM_DUTY_H	SEL_PWMDUTY[15:8]							R	0b 00000000	
99	SEL_PWM_DUTY_L	SEL_PWMDUTY[7:0]							R	0b 00000000	
9A	SCACTL	-	-	-	OUTDC_FI NJ	OUTDC_ EN	SCA_TEN[1:0]	SCA_TDA TA	R/W	0b 00000000	
9B	Reserved										
9C	SCAF_1	SCAFLT[8:1]							R	0b 00000000	
9D	SCAF_2	SCAFLT[16:9]							R	0b 00000000	
9E	SCAF_3	-	-	-	-	-	-	SCAFLT[18:17]	R	0b 00000000	
OTP-Registers											
AD	OTP_CTRL	p1	p0	Cmd[1:0]		Sel[3:0]				R/W	0b 00000000
AE	OTP_ST	-	-	-	-	-	FAIL	FINISH	BUSY	R	0b 00000000
AF	ECC_ST	-	IMD_2Err r ecc A	-	IMD_1Err_ ecc A	-	-	-	-	R	0b 00000000
OTP-A											
B0	DEFCONF	-	DEFFPS[2:0]		-	-		DEFDC_P WM	R/W	0b 00000000	
B1	DEFGCC	-	-	DEF_GCC[5:0]					R/W	0b 00000000	
B2	DEFTEMP_ SSCEN	-	DEFSSC EN	DEFSSC [1:0]		-	DEFTROF [2:0]		R/W	0b 00000000	
B3	DEFLED1	-	-	DEFLED[6:1]					R/W	0b 00000000	
B4	DEFLED2	-	-	DEFLED[12:7]					R/W	0b 00000000	
B5	DEFLED3	-	-	DEFLED[18:13]					R/W	0b 00000000	
B6	DEFPWM1	PWM2[3:0]			PWM1[3:0]				R/W	0b 00000000	
B7	DEFPWM2	PWM4[3:0]			PWM3[3:0]				R/W	0b 00000000	
B8	DEFPWM3	PWM6[3:0]			PWM5[3:0]				R/W	0b 00000000	
B9	DEFPWM4	PWM8[3:0]			PWM7[3:0]				R/W	0b 00000000	
BA	DEFPWM5	PWM10[3:0]			PWM9[3:0]				R/W	0b 00000000	
BB	DEFPWM6	PWM12[3:0]			PWM11[3:0]				R/W	0b 00000000	
BC	DEFPWM7	PWM14[3:0]			PWM13[3:0]				R/W	0b 00000000	
BD	DEFPWM8	PWM16[3:0]			PWM15[3:0]				R/W	0b 00000000	
BE	DEFPWM9	PWM18[3:0]			PWM17[3:0]				R/W	0b 00000000	
BF	ECC_A	ECCA							W	0b 00000000	
C0	W_PROTECT_A	WPROTECTA							W	0b 00000000	
FCh	OTP_UNLOCK	OTPUNLOCK							W	0b 00000000	

11.2 REGISTERS DEFINITION

11.2.1 00h CONFIG Register

ADDR	REG NAME	D7	D6:D4	D3:D2	D1	D0	DEFAULT
00h	CONFIG	-	PFS[2:0]	OFA[1:0]	PDE	DC_PWM	0b 00111110

PFS	PWM Frequency Setting
000	8bit, 31kHz, 8M
001	8+8bit, 31kHz, 8M
010	13+3bit, 976Hz, 8M
011	14+2bit, 488Hz, 8M(default)
100	16bit, 122Hz, 8M
101	16bit, 5Hz, 8M(for blink)
110	16bit, 2.5Hz, 8M(for blink)
111	16bit, 1.25Hz, 8M(for blink)

OFAx	“One Fail All On” or “One Fail All Fail” fault action mode setting
0X	“One Fail All Fail” (single LED short fault latches all outputs off, open or short auto recover)
10	“One Fail All Fail” (auto recover)
11	“One Fail All On”

PDE	Phase delay enable
0	Disable
1	Enable (6 groups phase delay)

DC_PWM	DC or PWM output select for all outputs
0	PWM dimming. PWM duty cycle is determined by PWM registers 26h~40h
1	DC output. PWM dimming is disabled, and all outputs are DC current (I_{OUTx})

11.2.2 01h GC_CTRL Register

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
01h	GC_CTRL	-	GCC [5:0]	0b 00111111

GCC and SCAX control the I_{OUT} as shown in following formula:

$$I_{OUT_F} = I_{OUT(MAX)} \times \frac{GCC}{63} \times \frac{SCAX}{127} \quad (5)$$

$$GCC = \sum_{n=0}^5 D[n] \cdot 2^n \quad (6)$$

$$SCAX = \sum_{n=0}^6 D[n] \cdot 2^n \quad (7)$$

11.2.3 02h TEMP_SEN Register

ADDR	REG NAME	D7:D3	D2:D0	DEFAULT
02h	TEMP_SEN	-	TROF [2:0]	0b 00000000

After adding analog dimming, the current of thermal roll off will not be a fixed proportion, and the slope of roll off can be calculated by formula. $I_{ROLL} = I_{set} * (V_{ADJ} - V_x) / 2$, (When $V_{ADJ} > 2V$, $I_{ROLL} = I_{set} * (2V - V_x) / 2$), I_{ROLL} is the current after roll off, I_{SET} is the current before roll off, V_{ADJ} is the voltage of the analog dimming pin, and V_x is the optional voltage (TROF bits) of the register.

TROF	Percentage of output current before thermal shutdown happens
000	0V
001	0.2V
010	0.4V
011	0.6V
100	0.8V
101	1.0V
110	1.2V
111	1.4V

11.2.4 03h~14h Scaling Registers

ADDR	REG NAME	D7	D6:D0	DEFAULT
03h	SCA1	-	SCA1_DATA [6:0]	0b 01111111
04h	SCA2	-	SCA2_DATA [6:0]	0b 01111111
05h	SCA3	-	SCA3_DATA [6:0]	0b 01111111
06h	SCA4	-	SCA4_DATA [6:0]	0b 01111111
07h	SCA5	-	SCA5_DATA [6:0]	0b 01111111
08h	SCA6	-	SCA6_DATA [6:0]	0b 01111111
09h	SCA7	-	SCA7_DATA [6:0]	0b 01111111
0Ah	SCA8	-	SCA8_DATA [6:0]	0b 01111111
0Bh	SCA9	-	SCA9_DATA [6:0]	0b 01111111
0Ch	SCA10	-	SCA10_DATA [6:0]	0b 01111111
0Dh	SCA11	-	SCA11_DATA [6:0]	0b 01111111
0Eh	SCA12	-	SCA12_DATA [6:0]	0b 01111111
0Fh	SCA13	-	SCA13_DATA [6:0]	0b 01111111
10h	SCA14	-	SCA14_DATA [6:0]	0b 01111111
11h	SCA15	-	SCA15_DATA [6:0]	0b 01111111
12h	SCA16	-	SCA16_DATA [6:0]	0b 01111111
13h	SCA17	-	SCA17_DATA [6:0]	0b 01111111
14h	SCA18	-	SCA18_DATA [6:0]	0b 01111111

The 7-bit Scaling Registers SCAx (03h~14h) individually set the DC output current of each channel.

GCC[5:0] and SCAx control the OUTx current (I_{OUTx}) as shown in following equation:

$$I_{OUTx} = I_{OUT_FU} \times \frac{GCC}{63} \times \frac{SCAx}{127} \quad (3)$$

Where x is from 1 to 18 for different output channel.

$$GCC = \sum_{n=0}^5 D[n] \cdot 2^n \quad (4)$$

$$SCAx = \sum_{n=0}^6 D[n] \cdot 2^n \quad (5)$$

11.2.5 15h~38h PWM Registers

ADDR	REG NAME	D7:D0	DEFAULT
15h	PWM1_H	PWM1_DATA [15:8]	0b 00000000
16h	PWM1_L	PWM1_DATA [7:0]	0b 00000000
17h	PWM2_H	PWM2_DATA [15:8]	0b 00000000
18h	PWM2_L	PWM2_DATA [7:0]	0b 00000000
19h	PWM3_H	PWM3_DATA [15:8]	0b 00000000
1Ah	PWM3_L	PWM3_DATA [7:0]	0b 00000000
1Bh	PWM4_H	PWM4_DATA [15:8]	0b 00000000
1Ch	PWM4_L	PWM4_DATA [7:0]	0b 00000000
1Dh	PWM5_H	PWM5_DATA [15:8]	0b 00000000
1Eh	PWM5_L	PWM5_DATA [7:0]	0b 00000000
1Fh	PWM6_H	PWM6_DATA [15:8]	0b 00000000
20h	PWM6_L	PWM6_DATA [7:0]	0b 00000000

21h	PWM7_H	PWM7_DATA [15:8]	0b 00000000
22h	PWM7_L	PWM7_DATA [7:0]	0b 00000000
23h	PWM8_H	PWM8_DATA [15:8]	0b 00000000
24h	PWM8_L	PWM8_DATA [7:0]	0b 00000000
25h	PWM9_H	PWM9_DATA [15:8]	0b 00000000
26h	PWM9_L	PWM9_DATA [7:0]	0b 00000000
27h	PWM10_H	PWM10_DATA [15:8]	0b 00000000
28h	PWM10_L	PWM10_DATA [7:0]	0b 00000000
29h	PWM11_H	PWM11_DATA [15:8]	0b 00000000
2Ah	PWM11_L	PWM11_DATA [7:0]	0b 00000000
2Bh	PWM12_H	PWM12_DATA [15:8]	0b 00000000
2Ch	PWM12_L	PWM12_DATA [7:0]	0b 00000000
2Dh	PWM13_H	PWM13_DATA [15:8]	0b 00000000
2Eh	PWM13_L	PWM13_DATA [7:0]	0b 00000000
2Fh	PWM14_H	PWM14_DATA [15:8]	0b 00000000
30h	PWM14_L	PWM14_DATA [7:0]	0b 00000000
31h	PWM15_H	PWM15_DATA [15:8]	0b 00000000
32h	PWM15_L	PWM15_DATA [7:0]	0b 00000000
33h	PWM16_H	PWM16_DATA [15:8]	0b 00000000
34h	PWM16_L	PWM16_DATA [7:0]	0b 00000000
35h	PWM17_H	PWM17_DATA [15:8]	0b 00000000
36h	PWM17_L	PWM17_DATA [7:0]	0b 00000000
37h	PWM18_H	PWM18_DATA [15:8]	0b 00000000
38h	PWM18_L	PWM18_DATA [7:0]	0b 00000000

Each OUTx has 16-bit (or 8+8-bit) to modulate the PWM duty cycle in 65536 steps.

The value of the PWM Registers decides the average current of each OUTx LED noted I_{LED} .

I_{LED} computed by following formula:

$$I_{OUTx_PWM} = I_{OUTx} \times D_{PWMx} \quad (6)$$

Where D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (16h~39h), in 16bit or 8+8-bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{15} D[n] \cdot 2^n}{65536} \quad (7)$$

In 8bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=8}^{15} D[n] \cdot 2^n}{256} \quad (8)$$

11.2.6 39h~41h Single LED Short Threshold Setting Registers

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
39h	LED1_2_SLS	LED2_SLSTH[3:0]	LED1_SLSTH [3:0]	0b 00000000
3Ah	LED3_4_SLS	LED4_SLSTH[3:0]	LED3_SLSTH [3:0]	0b 00000000
3Bh	LED5_6_SLS	LED6_SLSTH[3:0]	LED5_SLSTH [3:0]	0b 00000000
3Ch	LED7_8_SLS	LED8_SLSTH[3:0]	LED7_SLSTH [3:0]	0b 00000000

3Dh	LED9_10_SLS	LED10_SLSTH[3:0]	LED9_SLSTH [3:0]	0b 00000000
3Eh	LED11_12_SLS	LED12_SLSTH[3:0]	LED11_SLSTH [3:0]	0b 00000000
3Fh	LED13_14_SLS	LED14_SLSTH[3:0]	LED13_SLSTH [3:0]	0b 00000000
40h	LED15_16_SLS	LED16_SLSTH[3:0]	LED15_SLSTH [3:0]	0b 00000000
41h	LED17_18_SLS	LED18_SLSTH[3:0]	LED17_SLSTH [3:0]	0b 00000000

LEDx_SLSTH Single LED short threshold voltage

0000	2.5V
0001	3.2V
0010	3.9V
0011	4.6V
0100	5.3V
0101	6.0V
0110	6.7V
0111	7.4V
1000	8.1V
1001	8.8V
1010	9.5V
1011	10.2V
1100	11.4V
1101	12.6V
1110	13.8V
1111	15.0V

11.2.7 42h System Configuration Register (SYSCFG)

ADDR	REG NAME	D7	D6:D5	D4	D3:D1	D0	DEFAULT
42h	SYSCFG	SSCEN	SSC [1:0]	ACKEN	-	PWR	0b 00000000

ACKEN Acknowledge Enable

0	No acknowledge is transmitted following successfully received writes
1	Acknowledge (0x7F) is transmitted following successfully received writes

PWR This bit is reset to 0 upon power-up. It may be written to a 1 by the MCU. Reading this bit allows the MCU to detect if there has been a power cycle.

0	A power cycle has occurred since last write to a '1'
1	No power cycle has occurred since the last write to a '1'

SSCEN Spread Spectrum Enable

0	Disable
1	Enable-not allowed when PWM frequency is 244Hz

SSC Spread Spectrum frequency range

00	125Hz
01	250Hz
10	500Hz
11	1kHz

11.2.8 43h FS_FLTL Register

ADDR	REG NAME	D7	D6:D4	D3:D0	DEFAULT
43h	FS_FLTL	-	SHORT_FLT	FLT_UV	0b 00000100

FLT_UV set UVLO threshold VFLT_UV for the LED open fault detection and single LED short fault detection to prevent false fault triggering due to insufficient power supply voltage:

FLT_UV	UVLO threshold voltage for the LED open fault detection and single LED short fault detection
0000	4.5V
0001	5V
0010	6V
0011	7V
0100	8V (default)
0101	9V
0110	10V
0111	11V
1000	12V
1001	13V
1010	14V
1011	15V
1100	16V
1101	16V
1110	16V
1111	16V

SHORT_FLT	LED short threshold voltage
000	$V_{IN}-1V$
001	5V
010	6V
011	8V
100	10V
101	12V
110	14V
111	Not allowed

11.2.9 44h Diagnostic Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
44h	FLT_DET_EN	-	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	0b 00001111

SLSDF	Single LED Short Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

SLSDE	Single LED Short Detect Enable
0	Detect disabled
1	Detect enabled

SDF	Short Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

SDE	Short Detect Enable
0	Detect disabled
1	Detect enabled

ODF	Open Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

ODE Open Detect Enable
 0 Detect disabled
 1 Detect enabled

11.2.10 45h~4Eh Diagnostic Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
45h	FLT_CONFIG	-	SHCR	OPENCR	SLSHCR	FT[3:0]				0b 01100011
46h	SHORT_FLT1	-	-	SHORT_FLT[6:1]						0b 00000000
47h	SHORT_FLT2	-	-	SHORT_FLT[12:7]						0b 00000000
48h	SHORT_FLT3	-	-	SHORT_FLT[18:13]						0b 00000000
49h	OPEN_FLT1	-	-	OPEN_FLT[6:1]						0b 00000000
4Ah	OPEN_FLT2	-	-	OPEN_FLT[12:7]						0b 00000000
4Bh	OPEN_FLT3	-	-	OPEN_FLT[18:13]						0b 00000000
4Ch	SLS_FLT1	-	-	SLS_FLT[6:1]						0b 00000000
4Dh	SLS_FLT2	-	-	SLS_FLT[12:7]						0b 00000000
4Eh	SLS_FLT3	-	-	SLS_FLT[18:13]						0b 00000000

FT Fault report delay time setting
 0000 32us
 0001 64us
 0010 128us
 0011 256us(default)
 0100 512us
 0101 1.024ms
 0110 2.048ms
 0111 4.096ms
 1000 7.8125ms
 1001 15.625ms
 1010 31.25ms
 1011 62.5ms
 1100 0.125s
 1101 0.25s
 1110 0.5s
 1111 1s

SLSHCR single LED short output current reduce
 0 No reduce
 1 Output current reduced to 4mA (Typ.)

SHCR LED short output current reduce
 0 No reduce
 1 Output current reduced to 4mA (Typ.)

OPENCR LED OPEN output current reduce
 0 No reduce
 1 Output current reduced to 4mA (Typ.)

SHORT_FLTx LED string short fault flag for each OUT1~OUT18
 0 No LED string shorted
 1 LED string shorted

IS32LT3138A

OPEN_FLTx LED string open fault flag for each OUT1~OUT18
 0 No LED string open
 1 LED string open

SLS_FLTx Single LED short fault flag for each OUT1~OUT18
 0 No single LED shorted
 1 Single LED shorted

11.2.11 4Fh Fault Diagnostic Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
4Fh	FAULT_EN	ECC2F_EN	SCAF_EN	DUTYF_EN	TFE	CRCFE	RSET_OPE	RSET_SHE	TSDE	0b 11111111

ECC2F_EN ECC2 error Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

SCAF_EN SCA verification fail Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

DUTYF_EN PWM duty verification fail Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

TFE Thermal rolloff Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

CRCFE Interface communication Check Sum Failure Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

RSET_OPE ISET pin open Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

RSET_SHE ISET pin short Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

TSDE Thermal shutdown Report Enable at FAULTB pin
 0 Report disabled
 1 Report enabled

11.2.12 50h Fault Type Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
50h	FAULT_TYPE_1	-	CMWF2	CMWF1	TF	CRCF	RSET_OP	RSET_SH	TSD	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

CMWF2 Watch dog 2 Communication Time-Out fault flag
 0 No communication time-out
 1 Communication time-out

CMWF1	Watch dog 1 Communication Time-Out fault flag
0	No communication time-out
1	Communication time-out
TF	Thermal rolloff fault flag
0	No thermal rolloff
1	Thermal rolloff
CRCF	Interface communication Check Sum Failure fault flag
0	No communication Check Sum Failure
1	Communication Check Sum Failure
RSET_OP	ISET pin open fault flag (must to enable RSET_OPE (4Fh))
0	No open
1	Opened
RSET_SH	ISET pin short fault flag (must to enable RSET_SHE (4Fh))
0	No short
1	Shorted
TSD	Thermal shutdown fault flag
0	No thermal shutdown
1	Thermal shutdown

11.2.13 51h Fault Type Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
51h	FAULT_TYPE_2	SCAVF	LPBF	-	-	EXF	SLSHORTF	SHORTF	OPENF	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

SCAVF	SCA verification fault flag. Any output occurs SCA verification failure, this bit will set to "1".
0	No failure
1	Failure
LPBF	Loopback fault flag. Any output occurs loopback verification failure, this bit will set to "1".
0	No loopback failure
1	Loopback failure
EXF	external fault flag(must to enable One Fail All Fail(00h))
0	No faultb pin pulled down externally
1	Faultb pin pulled down externally
SLSHORTF	Single LED Short fault flag. Any out occurs single LED short, this bit will set to 1.
0	No single LED short
1	Single LED short
SHORTF	LED Short fault flag. Any out occurs LED short, this bit will set to 1.
0	No LED short
1	LED short
OPENF	LED Open fault flag. Any out occurs LED open, this bit will set to 1.
0	No LED open
1	LED open

11.2.14 52h Diagnostic Register (Continue)

ADDR	REG NAME	D7:D0	DEFAULT
52h	CERRCNT	CERRCNT [7:0]	0b 00000000

This register value is incremented each time a CRC error is received. This register may be read by the MCU and then written back to 0 to clear the count. The CERRCNT value saturates at FFh; it does not wrap back to 0 when it reaches FFh. The CERRCNT register is not automatically cleared when a communications reset is received. It must be cleared manually by writing it back to 0. Note that the CERRCNT register can be written to any 8-bit value. This is intended for diagnostic purposes.

11.2.15 53h Channel Special Function Register

ADDR	REG NAME	D7	D6	D5	D4	D3:D2	D1:D0	DEFAULT
53h	CH_FS	OUT18_FS	OUT17_FS	OUT16_FS	OUTADC_N	-	DCFB_N[1:0]	0b 00000000

This register can be used to set the reuse function of the Special pin. It should be noted that even if OUT16~OUT18 is set to the Special function through this register, after entering the Fail-safe mode, the Special Function pin will be set to LED OUT, and the Special Function will fail.

OUT16_FS OUT16 Function select
0 LED function
1 Disable LED function, set this pin for output(DCFB)

OUT17_FS OUT17 Function select
0 LED function
1 Disable LED function, Set this pin for ADC input

OUT18_FS OUT18 Function select
0 LED function
1 Disable LED function, Set this pin for ADC input

OUTADC_N OUT ADC Multiple select
0 8x(default)
1 2.2x

DCFB_N DCFB multiple selection of output current
00 disable
01 1x (The output current of each stage is 0.89μA, adjustable from 0μA to ±112.14μA)
10 2x (The output current of each stage is 1.78μA, adjustable from 0μA to ±224.28μA)
11 3x (The output current of each stage is 2.67μA, adjustable from 0μA to ±336.42μA)

11.2.16 54h DCFB Output Current Setting Register

ADDR	REG NAME	D7:D0	DEFAULT
54h	DCFB_OCS	DCFB_OUT[7:0]	0b 10000000

Pay attention when using DCFB Function, because After entering the Fail-safe mode, the Special Function pin will be set to LED OUT, Therefore, it is forbidden to enter Fail-Safe Mode 3 when using DCFB function. At the same time, if using Fail-Safe Mode 1, it is necessary to set DEFLED16 to LED off to avoid output pull current and lead to catastrophic failure of front-end DCDC.

DCFB_OUT DCFB Output Current Selection

0000 0000	0 μ A
0000 0001	0.89 μ A
0000 0010	1.78 μ A
0000 0011	2.67 μ A
0000 0100	3.56 μ A
0000 0101	4.45 μ A
.....	
0111 1101	111.25 μ A
0111 1110	112.14 μ A
0111 1111	113.03 μ A
1000 0000	0 μ A (default)
1000 0001	-0.89 μ A
1000 0010	-1.78 μ A
.....	
1111 1100	-110.36 μ A
1111 1101	-111.25 μ A
1111 1110	-112.14 μ A
1111 1111	-113.03 μ A

11.2.17 55h~58h ADC Input Channels Select Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
55h	CHSEL_1	CHSEL[7:0]								0b 00000000
56h	CHSEL_2	CHSEL[15:8]								0b 00000000
57h	CHSEL_3	CHSEL[23:16]								0b 00000000
58h	CHSEL_4	-	-	-	-	-	-	CHSEL[25:24]		0b 00000000

CHSELx ADC sampling channels select.

The ADC has fifteen multiplexed input channels (CH0~CH25) which can be respectively selected by the CHSEL[0]~CHSEL[25] bits. As below table. Multiple channels can be selected which will be periodically measured in turn.

Input Channel Select Bit	Channel No.	Input Signal	Setting
CHSEL[0]	CH0	V _{OUT1} or I _{OUT1}	"0" = Not Selected "1" = Selected
CHSEL[1]	CH1	V _{OUT2} or I _{OUT2}	
...	...	...	
CHSEL[17]	CH17	V _{OUT18} or I _{OUT18}	
CHSEL[18]	CH18	V _{REF}	
CHSEL[19]	CH19	V _{PTAT}	
CHSEL[20]	CH20	V _{DD}	
CHSEL[21]	CH21	V _{IN}	
CHSEL[22]	CH22	V _{ADJR}	
CHSEL[23]	CH23	V _{BG}	
CHSEL[24]	CH24	ADC_IN1(OUT 17)	
CHSEL[25]	CH25	ADC_IN2(OUT 18)	

11.2.18 59h ADC Configuration Register

ADDR	REG NAME	D7:D4	D3	D2:D1	D0	DEFAULT
59h	ADCCFG	OUT18_FCH[3:0]	OUT_SEL	ADCSH[1:0]	ADCEN	0b 00000000

OUT18_FCH OUT18 ADC follow Channel

0000 DC detect

0001 OUT1

0010 OUT2

... ..

1110 OUT14

1111 OUT15

OUT_SEL OUT ADC select

0 ADC detect Vout

1 ADC detect Iout

ADCSHx ADC sample/hold time setting

00/01 ADC sample/hold time = 4 ADC CLK (Default)

10 ADC sample/hold time = 8 ADC CLK

11 ADC sample/hold time = 16 ADC CLK

ADCEN ADC Enable

0 Disabled

1 Enabled

11.2.19 5Ah ADC Control Register

ADDR	REG NAME	D7	D6:D5	D4	D3:D2	D1	D0	DEFAULT
5Ah	ADCCTL	ADCCYC_F	-	ADCRST	-	LOOP	SADC	0b 00000010

ADCCYC_F ADC sampling finished flag (Read only)

0 ADC sampling in progress, ADC result is not valid

1 ADC sampling finished, ADC result is valid reading for host MCU

To get more stable and precise result, OUTx voltage is always sampled for 2 PWM cycles to calculate the average value.

To obtain stable and correct measurement results, in 8+8Bit PWM Mode, the maximum working threshold of ADC sampling is limited. Only when the PWM value is less than 0xFFF8(65528), ADC sampling and data update will be performed, otherwise it will be skipped, and the data will not be updated.

LOOP ADC sampling mode

0 ADC single conversion

1 Enable continue ADC conversion (Default)

SADC Start ADC measurement

0 ADC measurement stops (Default)

1 ADC measurement starts

Please set ADCEN bit at first, then set SADC bit, otherwise ADC cannot measure voltage.

ADCRST Reset all ADC result registers (5Bh~81h) to default value when ADC measurement starts

0 Not reset (Default)

1 Reset

11.2.20 5Bh~71h ADC Output detect Result Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
5Bh	ADC_OUT1_H	ADC_OUT1[9:2]								0b 00000000
5Ch	ADC_OUT2_H	ADC_OUT2[9:2]								0b 00000000
5Dh	ADC_OUT3_H	ADC_OUT3[9:2]								0b 00000000
5Eh	ADC_OUT4_H	ADC_OUT4[9:2]								0b 00000000
5Fh	ADC_OUT1_2_3_4_L	ADC_OUT4[1:0]	ADC_OUT3[1:0]	ADC_OUT2[1:0]	ADC_OUT1[1:0]	0b 00000000				
60h	ADC_OUT5_H	ADC_OUT5[9:2]								0b 00000000
61h	ADC_OUT6_H	ADC_OUT6[9:2]								0b 00000000
62h	ADC_OUT7_H	ADC_OUT7[9:2]								0b 00000000
63h	ADC_OUT8_H	ADC_OUT8[9:2]								0b 00000000
64h	ADC_OUT5_6_7_8_L	ADC_OUT8[1:0]	ADC_OUT7[1:0]	ADC_OUT6[1:0]	ADC_OUT5[1:0]	0b 00000000				
65h	ADC_OUT9_H	ADC_OUT9[9:2]								0b 00000000
66h	ADC_OUT10_H	ADC_OUT10[9:2]								0b 00000000
67h	ADC_OUT11_H	ADC_OUT11[9:2]								0b 00000000
68h	ADC_OUT12_H	ADC_OUT12[9:2]								0b 00000000
69h	ADC_OUT9_10_11_12_L	ADC_OUT12[1:0]	ADC_OUT11[1:0]	ADC_OUT10[1:0]	ADC_OUT9[1:0]	0b 00000000				
6Ah	ADC_OUT13_H	ADC_OUT13[9:2]								0b 00000000
6Bh	ADC_OUT14_H	ADC_OUT14[9:2]								0b 00000000
6Ch	ADC_OUT15_H	ADC_OUT15[9:2]								0b 00000000
6Dh	ADC_OUT16_H	ADC_OUT16[9:2]								0b 00000000
6Eh	ADC_OUT13_14_15_16_L	ADC_OUT16[1:0]	ADC_OUT15[1:0]	ADC_OUT14[1:0]	ADC_OUT13[1:0]	0b 00000000				
6Fh	ADC_OUT17_H	ADC_OUT17[9:2]								0b 00000000
70h	ADC_OUT18_H	ADC_OUT18[9:2]								0b 00000000
71h	ADC_OUT17_18_L	-	-	-	-	ADC_OUT18[1:0]	ADC_OUT17[1:0]	0b 00000000		

ADC_OUTx The ADC result of each OUTx pin voltage or current.

This result can be used to calculate the OUTx pin voltage by following equation:

$$V_{OUTx}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \times 8; (OUTADC_N = 0) \quad (9)$$

$$V_{OUTx}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \times 2.2; (OUTADC_N = 1) \quad (10)$$

This result can be used to calculate the OUTx pin current by following equation:

$$I_{OUTx}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5 \times \frac{100mA}{2} \quad (11)$$

11.2.21 72h~73h ADC Internal Reference Voltage Result Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
72h	ADC_VREF_H	ADC_VREF[9:2]								0b 00000000
73h	ADC_VREF_L	-	-	-	-	-	-	ADC_VREF[1:0]		0b 00000000

ADC_VREFx The ADC result of the internal reference voltage.

$$V_{REF}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \times 2 \quad (12)$$

11.2.22 74h~75h ADC PTAT Voltage Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
74h	ADC_VPTAT_H	ADC_VPTAT [9:2]								0b 00000000
75h	ADC_VPTAT_L	-	-	-	-	-	-	ADC_VPTAT [1:0]		0b 00000000

ADC_VPTATx The ADC result of internal PTAT voltage.

This result can be used to estimate the device junction temperature by following equation:

$$T_j(^{\circ}C) = \frac{\left(\frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2500 - 982 \right)}{3.752} + 25^{\circ}C \quad (13)$$

11.2.23 76h~77h ADC LDO Voltage Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
76h	ADC_VDD_H	ADC_VDD [9:2]								0b 00000000
77h	ADC_VDD_L	-	-	-	-	-	-	ADC_VDD [1:0]		0b 00000000

ADC_VDDx The ADC result of internal LDO voltage.

This result can be used to calculate the LDO voltage by following equation:

$$V_{VDD}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \times 5 \quad (14)$$

11.2.24 78h~79h ADC VIN Voltage Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
78h	ADC_VIN_H	ADC_VIN [9:2]								0b 00000000
79h	ADC_VIN_L	-	-	-	-	-	-	ADC_VIN [1:0]		0b 00000000

ADC_VINx The ADC result of VIN voltage.

This result can be used to calculate the VIN voltage by following equation:

$$V_{VIN}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \times 8 \quad (15)$$

11.2.25 7Ah~7Bh ADC ADJR Voltage Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
7Ah	ADC_VADJ_H	ADC_VADJ [9:2]								0b 00000000
7Bh	ADC_VADJ_L	-	-	-	-	-	-	ADC_VADJ [1:0]		0b 00000000

ADC_VADJx The ADC result of ADJR voltage.

This result can be used to calculate the ADJR voltage by following equation:

$$V_{VADJR}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \quad (16)$$

11.2.26 7Ch~7Dh ADC BG Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
7Ch	ADC_VBG_H	ADC_VBG [9:2]								0b 00000000
7Dh	ADC_VBG_L	-	-	-	-	-	-	ADC_VBG [1:0]		0b 00000000

ADC_VBGx The ADC result of internal BG voltage.

This result can be used to calculate the BG voltage by following equation:

$$V_{VBG}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \quad (17)$$

11.2.27 7Eh~81h ADC IN1 IN2 special input Result Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
7Eh	ADC_IN1_H	ADC_IN1 [9:2]								0b 00000000
7Fh	ADC_IN1_L	-	-	-	-	-	-	ADC_IN1 [1:0]		0b 00000000
80h	ADC_IN2_H	ADC_IN2 [9:2]								0b 00000000
81h	ADC_IN2_L	-	-	-	-	-	-	ADC_IN2 [1:0]		0b 00000000

ADC_VIN1 The ADC result of each OUT17 pin voltage.

This result can be used to calculate the OUT17 pin voltage by following equation:

$$V_{OUTx}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \quad (18)$$

ADC_VIN2 The ADC result of each OUT18 pin voltage.

This result can be used to calculate the OUT18 pin voltage by following equation:

$$V_{OUTx}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V; (\text{OUT18_FCH} = 0) \quad (19)$$

$$V_{OUTx}(V) = \frac{\sum_{n=0}^9 D[n] \cdot 2^n}{1024} \times 2.5V \times 2.2; (\text{OUT18_FCH} = 1) \quad (20)$$

11.2.28 82h Watchdog Timer 1 Register

ADDR	REG NAME	D7:D3	D2:D0	DEFAULT
82h	CMWT1	--	CMWTAP [2:0]	0b 00000011

CMWTAP [2:0] This 3-bit value selects the tap point (i.e., bit number, starting from 0) on the 24-bit communications watchdog timer to establish the time-out condition.

000	8ms
001	16ms
010	32ms
011	64ms(default)
100	128ms
101	256ms
110	512ms
111	1024ms

11.2.29 83h Watchdog Timer 2 Register

ADDR	REG NAME	D7	D6	D5:D3	D2:D0	DEFAULT
83h	CMWT2	-	WDT2CLR	WDT2_MAX[2:0]	WDT2_MIN[2:0]	0b 00011000

WDT2CLR WDT2 Counter Clear

Writing "1" to WDT2CLR clears the WDT2 count to 0. It is self-cleared by hardware.

WDT2MAX	with 8M clock
000	8ms
001	16ms
010	32ms
011	64ms(default)
100	128ms
101	256ms
110	512ms
111	1024ms

WDTMAX hold the timeout value for watchdog timer 2. When the counter reaches WDT2 timeout value, a fault flag is generated.

WDT2MIN	with 8M clock
000	8ms(default)
001	16ms
010	32ms
011	64ms
100	128ms
101	256ms
110	512ms
111	1024ms

WDTMIN hold the minimum value for watchdog timer 2. If WDT2 is cleared before reaching WDT2MIN, a fault flag is also generated.

11.2.30 90h LBIST State Register

ADDR	REG NAME	D7:D2	D1	D0	DEFAULT
90h	BSTSTA	-	FAIL	FINISH	0b 00000000

FINISH	LBIST state flag
0	LBIST in progress
1	LBIST finished

The device will do Logic Build in Self-test (LBIST) upon UVLO being released. When it is finished, this flag will be set to "1".

FAIL	LBIST result
0	Pass
1	Failure

This result is only available for check after LBIST being finished, FINISH bit set to "1". In case of LBIST result is failure, the device is defective and cannot be used.

11.2.31 91h Loopback Control Register

ADDR	REG NAME	D7:D6	D5	D4:D0	DEFAULT
91h	VFYCTL	MODE[1:0]	-	TOLERANCE[4:0]	0b 00000001

MODE	PWM loopback mode select
00	Disabled loop back
01	PWM look back self-check, Check result(96h~97h) mandatory 0xFFFF
10	PWM look back self-check, Check result(96h~97h) mandatory 0x0000
11	PWM look back test enable

TOLERANCEx Loopback comparison tolerance setting

Preset PWM duty cycle deviation tolerance between the measurement result and the PWM duty cycle setting value in the PWM buffer.

$$Tolerance = \sum_{n=0}^4 D[n] \cdot 2^n \times 4 + 3 \quad (21)$$

11.2.32 92h Loopback Configuration Register

ADDR	REG NAME	D7	D6:D5	D4:D0	DEFAULT
92h	VFYCFG	START/BUSY	-	VFYCHSEL[4:0]	0b 00000000

START/BUSY Loopback verification state flag (write 1 only and auto hardware clear when complete LB test)

0 invalid

1 start LB test

VFYCHSELx Loopback verification channel select

00000 PWM signal from output stage of OUT1

00001 PWM signal from output stage of OUT2

00010 PWM signal from output stage of OUT3

.....

01111 PWM signal from output stage of OUT16

10000 PWM signal from output stage of OUT17

10001 PWM signal from output stage of OUT18

Other Invalid

The PWM duty cycle loopback verification circuit has eighteen multiplexed inputs to monitor the PWM duty cycle of output channels. The eighteen input channels (LBTCH1~LBTCH18) are respectively connected to each current source output stage. Only one channel can be verified at a time.

To obtain stable and correct measurement results, the Loopback module sets the working range limit. Only when the PWM setpoint is within the working range, it will be judged and reported by line sampling and Fault, otherwise the data will not be updated. Different PWM modes have different range limits, as shown in the table below.

To ensure the reliability of the measurement results, the output current of the channel should not be less than 1mA when using Loopback to measure the output. It is recommended to use 16Bit PWM mode when Loopback module self-test to ensure the correctness of the Loopback module.

Loopback Working Range Limit Table

PWM Mode	Minimum PWM value (DEC)	Maximum PWM value (DEC)
8Bit Mode	10	245
8+8 Mode	2112	63423
13+3Bit Mode	80	65455
14+2Bit Mode	36	65499
16Bit Mode	10	65525

11.2.33 93h~95h Loopback Fault Flag Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
93h	DUTYF_1	DUTYFLT[8:1]								0b 00000000
94h	DUTYF_2	DUTYFLT[16:9]								0b 00000000
95h	DUTYF_3	-	-	-	-	-	-	DUTYFLT[18:17]		0b 00000000

DUTYFLT_x Loopback fault flag for each OUT1~OUT18

0 No loopback failure

1 Loopback failure

11.2.34 96h~97h Loopback PWM Duty Cycle Result Registers

ADDR	REG NAME	D7:D0	DEFAULT
96h	PWMDUTY_H	PWMDUTY[15:8]	0b 00000000
97h	PWMDUTY_L	PWMDUTY[7:0]	0b 00000000

PWMDUTYx The PWM duty cycle measure result of the selected channel.

11.2.35 98h~99h Select PWM Duty Cycle Registers

ADDR	REG NAME	D7:D0	DEFAULT
98h	SEL_PWMDUTY_H	SEL_PWMDUTY[15:8]	0b 00000000
99h	SEL_PWMDUTY_L	SEL_PWMDUTY[7:0]	0b 00000000

SEL_PWMDUTYx The PWM duty cycle of the selected channel.

11.2.36 9Ah SCA verification Control Register

ADDR	REG NAME	D7:D5	D4	D3	D2:D1	D0	DEFAULT
9Ah	SCACTL	-	OUTDC_FINJ	OUTDC_EN	SCA_TEN[1:0]	SCA_TDATA	0b 00000000

OUTDC_FINJ ADC IOUT detect verification function enable

0 Disabled

1 Enabled DC IOUT detect verification 15mA

OUTDC_EN ADC IOUT detect enable

0 Disabled

1 Enabled

SCA_TEN SCA verification function enable

00 Disabled

01/10 SCA verification Enable real-time

11 Enable SCA bit comparison

SCA_TDATA SCA bit comparison data

When SCA verification function, the SCA registers(03h~14h) only one bit can be set as '1'.(loop 1~8 times)

11.2.37 9Ch~9Eh SCA Fault Flag Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
9Ch	SCAF_1	SCAFLT[8:1]								0b 00000000
9Dh	SCAF_2	SCAFLT[16:9]								0b 00000000
9Eh	SCAF_3	-	-	-	-	-	-	SCAFLT[18:17]		0b 00000000

DUTYFLT_x SCA bit fault flag for each OUT1~OUT18

0 No failure

1 Failure

11.2.38 ADh OTP Control Register

ADDR	REG NAME	D7	D6	D5:D4	D3:D0	DEFAULT
ADh	OTP_CTRL	p1	p0	Cmd[1:0]	Sel[3:0]	0b 00000000

There are four select OTP ZoneX bits, two OTP operation bits and two parity bits.

The parity bits for the OTP control byte are calculated with the equations below:

$p[1] = \sim(\text{Sel}[1] \wedge \text{Sel}[3] \wedge \text{Cmd}[0] \wedge \text{Cmd}[1])$
 $p[0] = \text{Sel}[0] \wedge \text{Sel}[1] \wedge \text{Sel}[2] \wedge \text{Cmd}[0]$

Cmd Comand Select
 01 OTP write operation
 11 OTP read operation
 Others Not allow

Sel Zone Select
 0001 select OTP Zone A
 Others Not allow

11.2.39 AEh OTP Status Register

ADDR	REG NAME	D7:D3	D2	D1	D0	DEFAULT
AEh	OTP_ST	-	FAIL	FINISH	BUSY	0b 00000000

FAIL OTP write fail
FINISH OTP write finish
BUSY OTP operation in progress

11.2.40 AFh ECC Status Register

ADDR	REG NAME	D7	D6	D5	D4	D3:D0	DEFAULT
AFh	ECC_ST	-	IMD_2Err_ecc A	-	IMD_1Err_ecc A	-	0b 00000000

IMD_2Err_ecc A ECC detects 2bit or more errors
IMD_1Err_ecc A ECC detected 1bit error

11.2.41 B0h DEFCONFIG Register (fail safe mode 1)

ADDR	REG NAME	D7	D6:D4	D3:D1	D0	DEFAULT
B0h	DEFCONF	-	DEFPFS[2:0]	-	DEFDC_PWM	0b 00000000

DEFPFS PWM Frequency Setting
 000 31kHz, 8M
 001 31kHz, 8M
 010 976Hz, 8M
 011 488Hz, 8M
 100 122Hz, 8M
 101 5Hz, 8M (for blink)
 110 2.5Hz, 8M (for blink)
 111 1.25Hz, 8M (for blink)

DEFDC_PWM DC or PWM output select for all outputs
 0 PWM dimming. PWM duty cycle is determined by PWM registers B6h~BEh
 1 DC output. PWM dimming is disabled, and all outputs are DC current (I_{OUTX})

11.2.42 B1h DEFGCC Register (fail safe mode 1)

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
B1h	DEFGCC	-	DEFGCC [5:0]	0b 00000000

DEFGCC controls the I_{OUT} as shown in following formula:

$$I_{OUT_F} = I_{OUT(MAX)} \times \frac{GCC}{63} \quad (22)$$

$$GCC = \sum_{n=0}^5 D[n] \cdot 2^n \quad (23)$$

11.2.43 B2h DEFCONFIG Register (fail safe mode 1)

ADDR	REG NAME	D7	D6	D5:D4	D3	D2:D0	DEFAULT
B2h	DEFTEMP_SSCEN	-	DEFSSCEN	DEFSSC [1:0]	-	DEFTROF [2:0]	0b 00000000

After adding analog dimming, the current of thermal roll off will not be a fixed proportion, and the slope of roll off can be calculated by formula. $I_{ROLL} = I_{set} \times (V_{ADJ} - V_x) / 2$, (When $V_{ADJ} > 2V$, $I_{ROLL} = I_{set} \times (2V - V_x) / 2$), I_{ROLL} is the current after roll off, I_{SET} is the current before roll off, V_{ADJ} is the voltage of the analog dimming pin, and V_x is the optional voltage (TROF bits) of the register.

EDFTROF Percentage of output current before thermal shutdown happens

000	0V
001	0.2V
010	0.4V
011	0.6V
100	0.8V
101	1.0V
110	1.2V
111	1.4V

DEFSSCEN Spread Spectrum Enable

0	Disable
1	Enable-not allowed when PWM frequency is 244Hz

DEFSSC Spread Spectrum frequency range

00	125Hz
01	250Hz
10	500Hz
11	1kHz

11.2.44 B3h~B5h DEFLED Register (Fail Safe Mode 1)

ADDR	REG NAME	D7:D6	D5	D4	D3	D2	D1	D0	DEFAULT
B3h	DEFLED1	-	DEFLED6	DEFLED5	DEFLED4	DEFLED3	DEFLED2	DEFLED1	0b 00000000
B4h	DEFLED2	-	DEFLED12	DEFLED11	DEFLED10	DEFLED9	DEFLED8	DEFLED7	0b 00000000
B5h	DEFLED3	-	DEFLED18	DEFLED17	DEFLED16	DEFLED15	DEFLED14	DEFLED13	0b 00000000

DEFLEDx LED State Bit

0	LED off
1	LED on

11.2.45 B6h~BEh DEFPWM Register (Fail Safe Mode 1)

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
B6h	DEFPWM1	PWM2[3:0]	PWM1[3:0]	0b 00000000
B7h	DEFPWM2	PWM4[3:0]	PWM3[3:0]	0b 00000000
B8h	DEFPWM3	PWM6[3:0]	PWM5[3:0]	0b 00000000
A9h	DEFPWM4	PWM8[3:0]	PWM7[3:0]	0b 00000000
BAh	DEFPWM5	PWM10[3:0]	PWM9[3:0]	0b 00000000
BBh	DEFPWM6	PWM12[3:0]	PWM11[3:0]	0b 00000000
BCh	DEFPWM7	PWM14[3:0]	PWM13[3:0]	0b 00000000
BDh	DEFPWM8	PWM16[3:0]	PWM15[3:0]	0b 00000000
BEh	DEFPWM9	PWM18[3:0]	PWM17[3:0]	0b 00000000

Each OUTx has 4-bit to modulate the PWM duty cycle in 16 steps.

The value of the PWM Registers decides the average current of each OUTx LED noted I_{LED} .

I_{LED} computed by following formula:

$$I_{OUTx_PWM} = I_{OUTx} \times D_{PWMx} \quad (24)$$

Where D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (16h~39h),

In 4bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^3 D[n] \cdot 2^n}{16} \quad (25)$$

11.2.46 BFh ECC A Register

ADDR	REG NAME	D7:D0	DEFAULT
BFh	ECC_A	ECCA	0b 00000000

Data check byte 0xB0~0xBE.

11.2.47 C0h Write Protect area A Register

ADDR	REG NAME	D7:D0	DEFAULT
C0h	W_PROTECT_A	WPROTECTA	0b 00000000

OTP-A data protect byte, it must be written 0xFF.

11.2.48 FCh OTP Write Unlock Register

ADDR	REG NAME	D7:D0	DEFAULT
FCh	OTP_UNLOCK	OTPUNLOCK	0b 00000000

OTP register unlock byte, unlock OTP registers(B0h~C0h)

Write 0xA5->0x69 unlock OTPA, other lock OTPA.

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12 CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

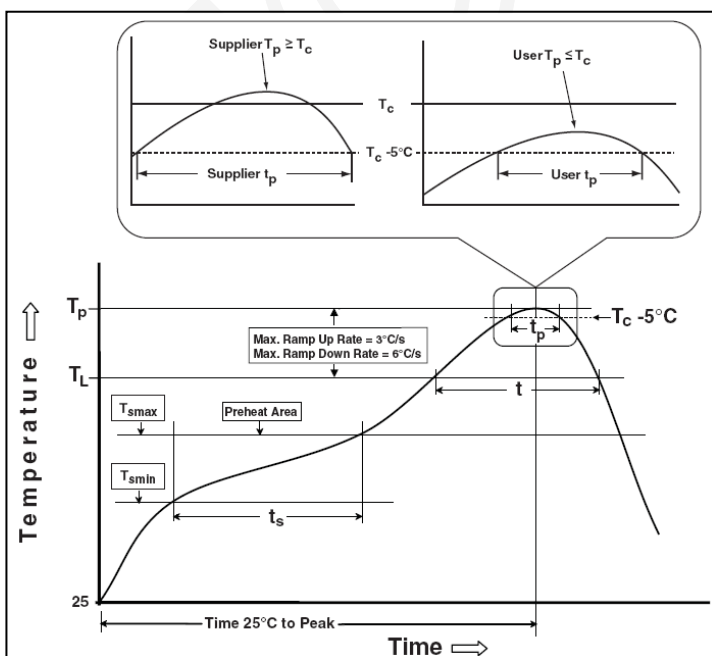
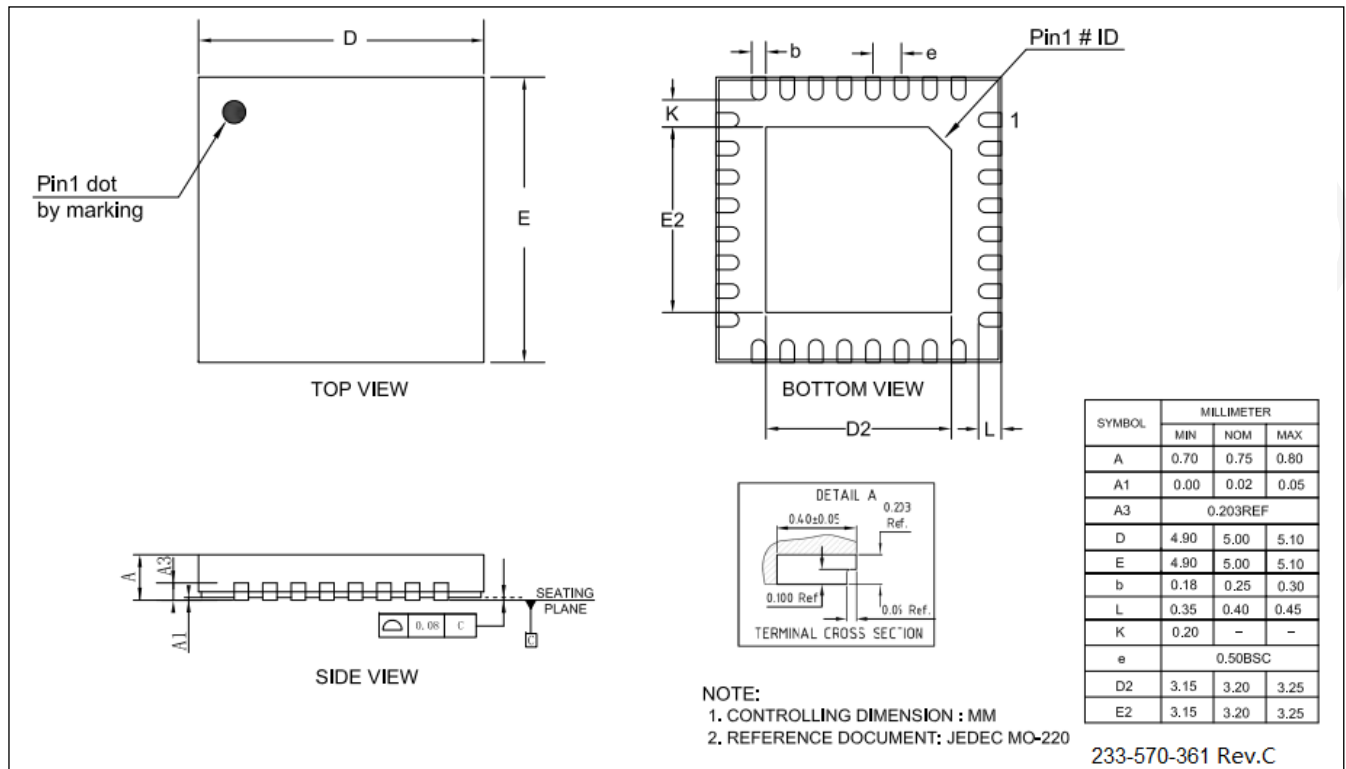


Figure 23 Classification Profile

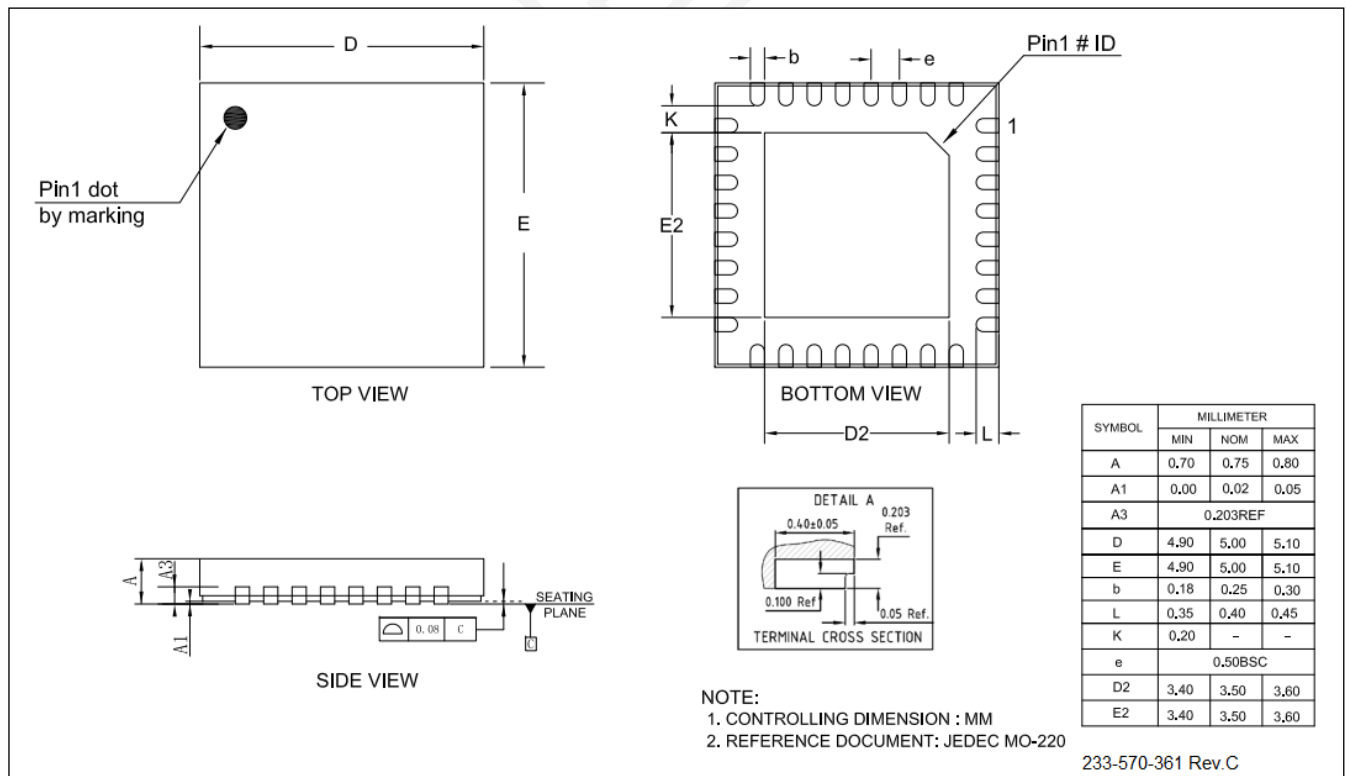
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13 PACKAGE INFORMATION

WFQFN-32 (IS32LT3138A-QWLA3-TR)



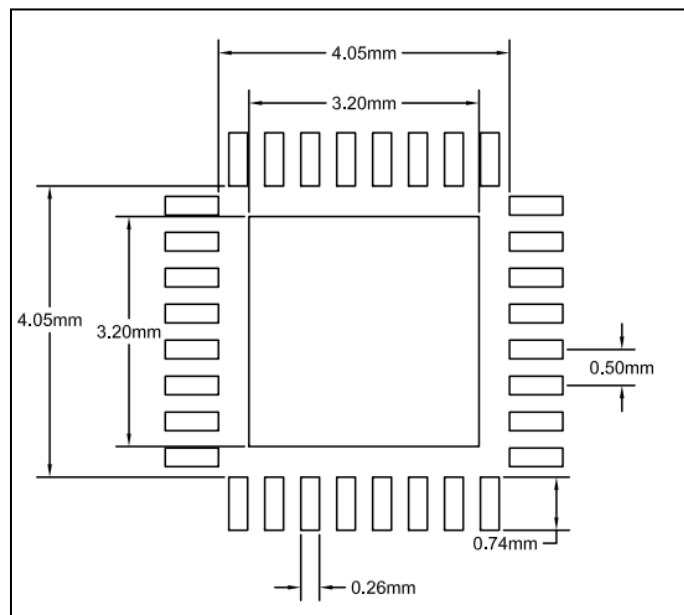
WFQFN-32 (IS32LT3138A-QWLCA3-TR) (with copper wire bonding)



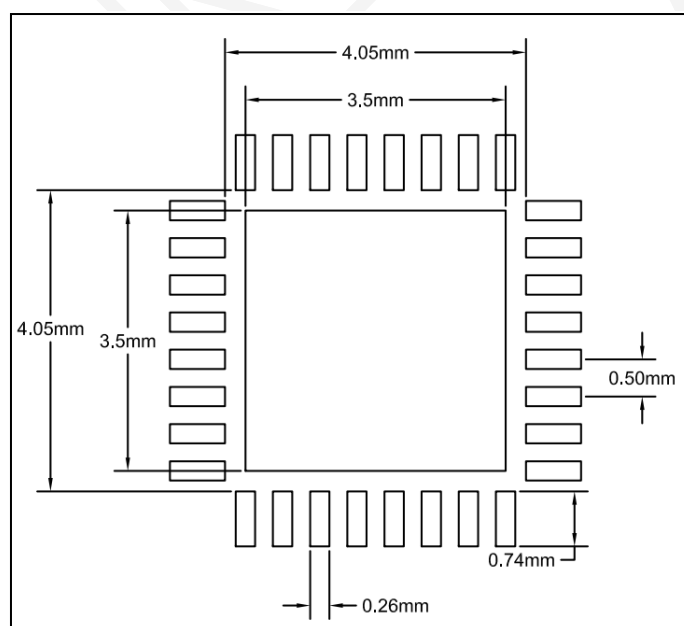
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14 RECOMMENDED LAND PATTERN

WFQFN-32 (IS32LT3138A-QWLA3-TR)



WFQFN-32 (IS32LT3138A-QWLC3-TR) (with copper wire bonding)



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

15 REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2024.03.21
A	Release to Mass-Production	2024.12.16
B	1. Update the function description for the FAULT section 2. Fix the description error 3. Optimize the code format 4. Revise θ_{JP} to θ_{JC_BOT}	2026.01.04