IS32LT3137

12 CHANNELS, LINEAR LED DRIVER WITH UART INTERFACE

May 2024

1 GENERAL DESCRIPTION

The IS32LT3137 is a linear programmable current regulator consisting of 12 output channels capable of up to 100mA each. It has a UART interface compatible with CANFD PHY for communication with a master microcontroller or ECU. It uses a command and response protocol mastered by the host microcontroller to read and write the registers to and from one or multiple IS32LT3137 devices.

Each output can individually support 12-bit PWM dimming and 7-bit DC current adjustment. The outputs can be combined to provide higher current drive capability to max 1.2A.

For added system reliability, the IS32LT3137 integrates fault detection circuitry for open/short string, single LED short, and over temperature conditions. Faults are recorded in registers which can be accessed by an external MCU. To optimize EMI performance, the IS32LT3137 features spread spectrum on the internal PWM and LED channel outputs have programmable slew rate control and phase delay to mitigate EMI and power supply inrush current.

The IS32LT3137 is targeted at the automotive market such as interior accent lighting and exterior tail lighting. It is offered in WFQFN-32 (5mm×5mm) package.

2 APPLICATIONS

- Animation Rear Light
- Animation Tail Light
- Animation Daytime Running Light

3 FEATURES

- Wide input voltage supply from 4.5V to 16V
- Maximum output voltage 16V
- UART Communication Interface
  - UART interface compatible with CANFD physical layer, 1MHz maximum.
  - UART communication with CRC to ensure robustness of communication
  - Support up to max. 16 addressable devices
  - Watch dog timer
  - Support Fail safe mode
- 12 channels capable of 100mA each
  - ±4.5% @ 100mA bit-to-bit output current mismatch
  - ±5% @ 100mA device-to-device output current accuracy
- Combined for higher current capability with same current accuracy
  - Minimum headroom voltage of 0.5V (Max.) at 100mA
- Individual PWM dimming to each channel
  - 4096 steps (12-bit) PWM duty cycle setting
    - 7+5-bit at 24kHz
    - 12-bit at 244Hz
    - 8-bit at 24kHz
  - Phase delay minimizes inrush current (4 groups)
- Slew rate control and spread spectrum optimize EMI performance
- 64 steps (6-bit) global current setting
- Individual 128 steps (7-bit) DC current adjustment to each channel
- DC Binning support (ADJR pin)
- Fault protection with reporting
  - Fail safe modes selection
  - LED string open/short detect
  - Single LED short detect
  - Programmable fault reporting delay time
  - Programmable over temperature current roll off
  - Thermal shutdown
  - CRC error detection
  - ISET short to GND
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- Operating temperature range (-40°C ~ +125°C)
- WFQFN-32 (5mm×5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

4 TYPICAL APPLICATION CIRCUIT

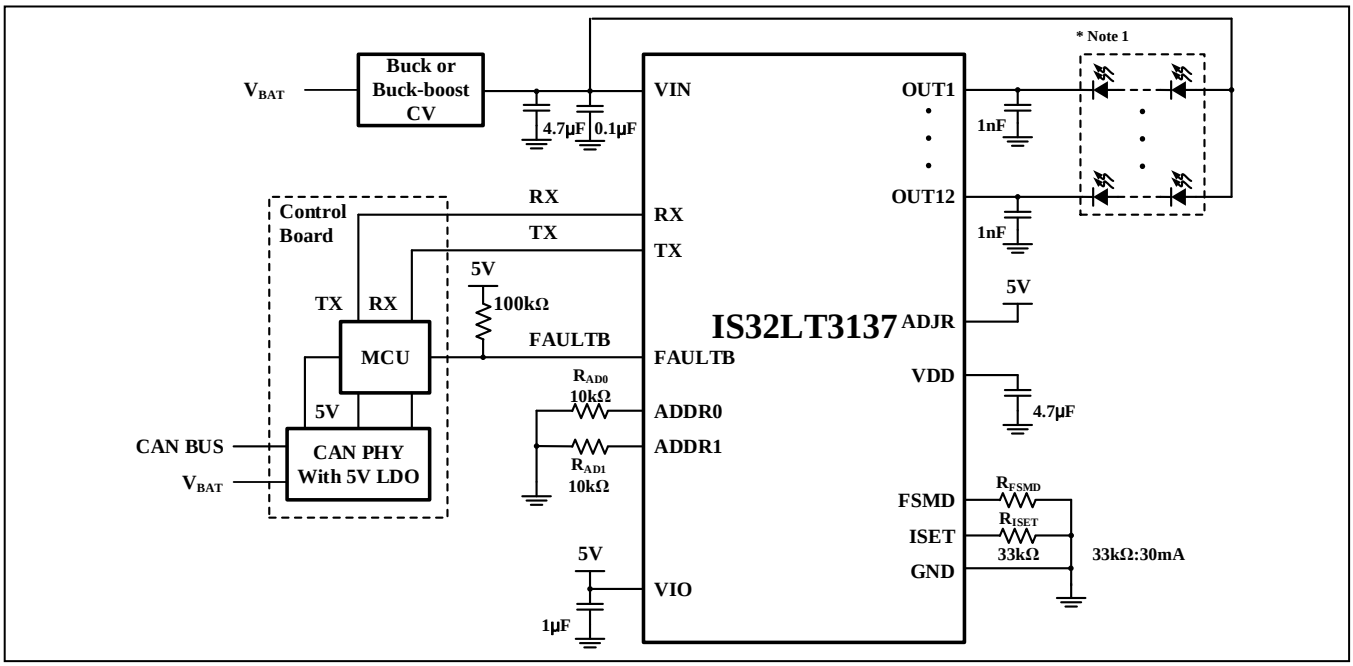


Figure 1 Typical Application Circuit of IS32LT3137 with UART Interface

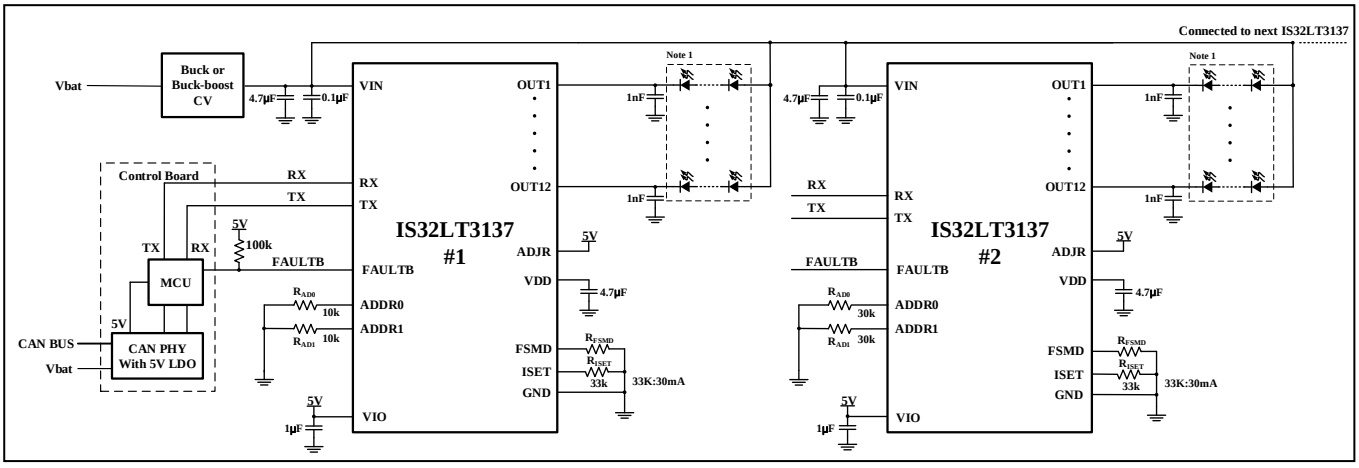


Figure 2 Typical Application Circuit of Multiple IS32LT3137 with UART Interface

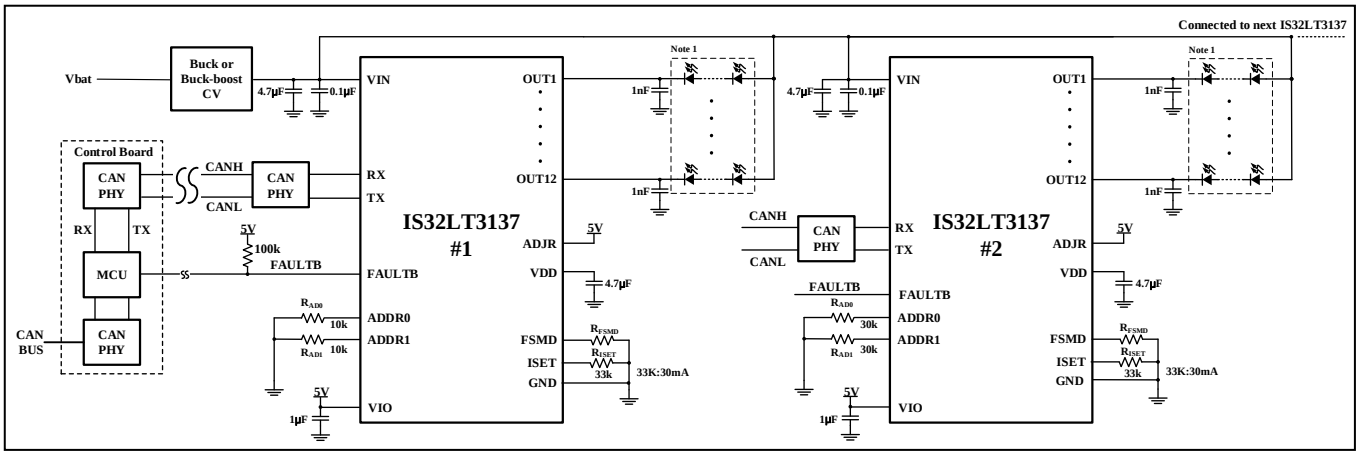
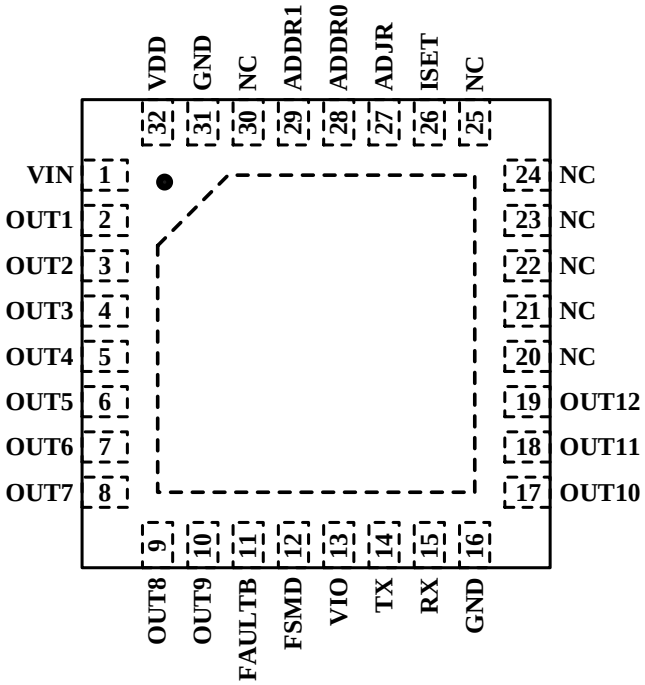


Figure 3 Typical Application Circuit of Multiple IS32LT3137 with External CAN Transceiver for Off-board Long Distance Communication

Note 1: The forward voltage variation of output channels (OUTx) should be kept as smaller as possible to minimize the heat consumption on device and prevent false fault triggering.

5 PIN CONFIGURATION

Package	Pin Configuration (Top View)
WFQFN-32	

DESCRIPTION

No.	Pin	Description
1	VIN	Power supply input.
2~10, 17~19	OUT1~OUT12	Current sink channels.
11	FAULTB	Open drain fault reporting pin. FAULTB pin is open drain output and requires an external pull-up resistor.
12	FSMD	Connect resistor to GND to select fail safe mode.
13	VIO	For TX power supply
14	TX	UART interface transmitted data pin.
15	RX	UART interface received data pin.
16, 31	GND	Ground.
20~25, 30	NC	No connection. Pin 30 should be left floating, do not connect to GND or any other pins or signals.
26	ISET	Input pin used to connect an external resistor to set the global output current.
27	ADJR	For analog dimming control
28~29	ADDR0~ADDR1	Address setting. Connect different values resistors from these pins to GND to assign device address.
32	VDD	4.2V LDO output. Connect a 4.7μF X7R capacitor to GND.
	Thermal Pad	Must be connected to GND. Connect thermal pad to external GND plane on board for better thermal performance.

6 ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3137-QWLA3-TR IS32LT3137-QWLCA3-TR (Note 2)	WFQFN-32, Lead-free	2500

Note 2: IS32LT3137-QWLCA3-TR is with copper wire bonding.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{IN}	-0.3V ~ 20.0V
Voltage at TX, RX, ADDRx, ISET, VDD, VIO, ADJR, FSMD	-0.3V ~6V
Voltage at OUT1 to OUT12, FAULTB	+20V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	39.7°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-2A), θ_{JP}	2.167°C/W
ESD (HBM) ESD (CDM)	±2.5kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ELECTRICAL CHARACTERISTICS

V_{IN}= 12V, T_J= T_A= 25°C, unless otherwise noted. (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage		4.5		16	V
I_{OUT}	Maximum output current	R_{ISET}= 10kΩ, GCC= 0x3F, SCAx= 0x7F, PWM= 0xFFF	93.5	100	106.5	mA
	Output current	R_{ISET}= 33kΩ, GCC= 0x3F, SCAx= 0x7F, PWM= 0xFFF	27.9	30	32.1	mA
ΔI_{MAT}	I_{OUT} mismatch (bit to bit) (Note 4)	I_{OUT}= 30mA	-6.5		6.5	%
		I_{OUT}= 100mA	-4.5		4.5	%
ΔI_{OUT}	I_{OUT} accuracy (device to device) (Note 5)	I_{OUT}= 30mA	-5		5	%
		I_{OUT}= 100mA	-5		5	%
V_{HR}	Headroom voltage	I_{OUT}= 100mA		0.34	0.5	V
		I_{OUT}= 30mA		0.2	0.4	V
I_{CC}	Quiescent power supply current	R_{ISET}= 33kΩ, GCC= 0x3F, SCAx= 0x7F, PWM= 0	3	4.5	6.5	mA
V_{ISET}	ISET voltage	R_{ISET}= 10kΩ, GCC= 0x3F, SCAx= 0x7F, PWM= 0xFFF	1.94	2.0	2.06	V
I_{OZ}	Output leakage current	PWM= SL= GCC= 0, V_{OUT}= 16V			1	μA
f_{OUT}	PWM frequency of output	Frequency setting= 24kHz, 8bit PWM mode	21.6	24	26.4	kHz
		Frequency setting= 24kHz, 7+5bit PWM mode, PWM>31/4096	21.6	24	26.4	kHz
		Frequency setting= 244Hz, 12bit PWM mode	219	244	269	Hz

ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 12V, T_J= T_A= 25°C, unless otherwise noted. (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{SD}	Thermal shutdown			168		°C
T_{SD_HYS}	Thermal shutdown hysteresis			15		°C
V_{PD_FAULTB}	FAULTB pin pull-down capability	I_{SINK}= 2mA		0.1	0.2	V
I_{LKG_FAULTB}	FAULTB pin leakage current	$V_{PULL-UP}$= 16V			1	μA
V_{IH_RX}	Logic “1” input voltage		2			V
V_{IL_RX}	Logic “0” input voltage				0.7	V
$V_{OL(TX)}$	Low level output voltage	I_{SINK}= 5mA			0.3	V
$V_{OH(TX)}$	High level output voltage	I_{SOURCE}=5mA	V_{IO}-0.3		V_{IO}	V
$V_{TH1\_AD/FS}$	ADDR0/ADDR1/FSMD threshold1		0.9	1	1.1	V
$V_{TH2\_AD/FS}$	ADDR0/ADDR1/ FSMD threshold2		1.85	2	2.15	V
$V_{TH3\_AD/FS}$	ADDR0/ADDR1/ FSMD threshold3		2.8	3	3.2	V
$I_{AD/FS}$	ADDR/FS source current		46	50	54	μA
V_{SC_FL}	LED string short detection falling threshold	R_{ISET}=33kΩ, GCC=0x3F, SCAx= 0x7F, PWM=0xFFF, measured at V_{IN}-V_{OUTx} SHORT_FLT(4Bh) = “000”	0.5	1		V
V_{SC_RS}	LED string short detection rising threshold	R_{ISET}=33kΩ, GCC=0x3F, SCAx= 0x7F, PWM=0xFFF, measured at V_{IN}-V_{OUTx} SHORT_FLT(4Bh) = “000”		1.2		V
V_{OC_FL}	LED string open detection falling threshold	R_{ISET}=33kΩ, GCC=0x3F, SCAx= 0x7F, PWM=0xFFF, measured at OUTx	50	100		mV
V_{OC_RS}	LED string open detection rising threshold	R_{ISET}=33kΩ, GCC=0x3F, SCAx= 0x7F, PWM=0xFFF, measured at OUTx		167		mV
V_{DD}	LDOOUT output voltage		4.08	4.2	4.32	V
I_{DD_MAX}	LDOOUT output current capability	V_{IN}> 4.5V, V_{DD}> 3.8V			50	mA
I_{DD_LIM}	LDOOUT output current limit	V_{IN}= 12V, V_{DD}= 0V	60			mA
V_{DD_UV}	LDOOUT undervoltage-lockout threshold	Voltage falling, IC disabled		3.7		V
V_{DD_UVHY}	VDD undervoltage-lockout hysteresis			100		mV

ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 12V, T_J= T_A= 25°C, unless otherwise noted. (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ΔI_{ICTRL_1}	I_{OUT} mismatch (bit to bit)	V_{ADJ} = 0.6V	-3		3	%
ΔI_{ICTRL_2}		V_{ADJ} = 1.4V	-3		3	%
V_{SLSTH}	Single LED short detect threshold	SLSTH (41h~49h) = “0010”		3.9		V
V_{F_UVLO}	Single LED short/String open detect UVLO	FS_FLTL (4Bh) = “00000100”		8		V
V_{IO}	TX power supply		3		5.5	V
V_{VIN_UV}	VIN undervoltage-lockout threshold	Voltage falling, IC disable		3.7		V
V_{VIN_UVHY}	VIN undervoltage-lockout hysteresis			100		mV
f_{OSC}	System clock frequency		32.34	33	33.66	MHz

Note 4: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = MAX\left(ABS\left(\frac{I_{OUTn}(n = 1\sim12)}{\frac{I_{OUT1} + I_{OUT2} + \cdots + I_{OUT12}}{12}} - 1 \right) \right) \times 100\%$$

Note 5: I_{OUT} accuracy (device to device) $\triangle I_{OUT}$ is calculated:

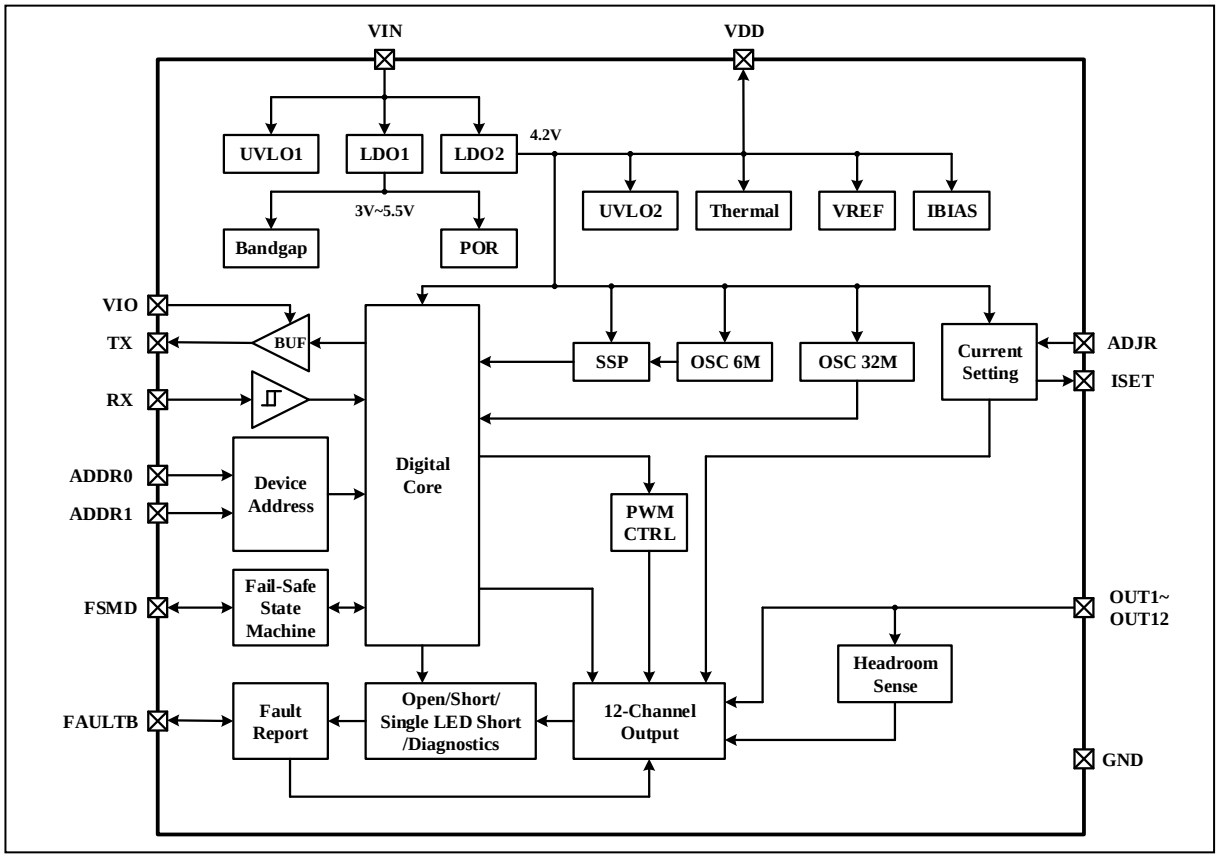
$$\Delta I_{OUT} = ABS\left(\frac{\frac{I_{OUT1} + I_{OUT2} + \cdots + I_{OUT12}}{12} - I_{OUT(TYP)}}{I_{OUT(TYP)}} \right) \times 100\%$$

When R_{ISET}=10kΩ, $I_{OUT(TYP)}$ = 100mA; and when R_{ISET}=33kΩ, $I_{OUT(TYP)}$ = 30mA.

Note 6: Production testing of the device is performed at 25°C.

Note 7: Guaranteed by design.

8 FUNCTIONAL BLOCK DIAGRAM



9 APPLICATION INFORMATION

9.1 OVERVIEW

The IS32LT3137 is an automotive 12-channel LED driver with a UART interface for individual control of each LED string. Each channel is a constant current sink capable of up to 100mA and supports both DC adjustment and PWM dimming. The output current and PWM duty cycle of each channel can be individually configured through the UART interface. For high current LED applications, multiple output channels can be combined in parallel.

For added system reliability, the IS32LT3137 features various fault protections, including LED string open, LED string shorted, single LED shorted, overcurrent (ISET pin shorted), over temperature, CRC error and watchdog timeout (fail-safe modes) conditions for robust operation. Detection of these failures is reported by a dedicated reporting pin, FAULTB. There are also dedicated flag bits in registers for each failure which can be read back by the external host MCU through the interfaces. To optimize EMI performance, the IS32LT3137 features spread spectrum on the internal PWM base clock to spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. In addition, the output current source ON/OFF transitions during PWM dimming have a slew rate control and programmable phase delay to mitigate EMI and power supply inrush current.

The IS32LT3137 interface is UART, and it supports up to 16 slave IS32LT3137 devices. The device address can be configured by the three address pins. The UART receives data to control all output channels and sends back fault information to the host MCU. The UART interface in conjunction with an external standard CAN transceiver enables long distance communication with a host MCU placed outside of the lamp module (as shown in Figure 4). Based on the CAN physical layer, it achieves excellent EMC and EMI performance. The embedded CRC correction of the UART data stream can ensure robust communication in automotive environments. The UART interface is easily supported by most MCUs in the market.

To further increase robustness, the fail-safe mode of the device allows automatic switching to fail-safe state in case of the communication loss, for example, host MCU failure or communication cables broken. The device supports different fail-safe modes configured by the FSMD pin.

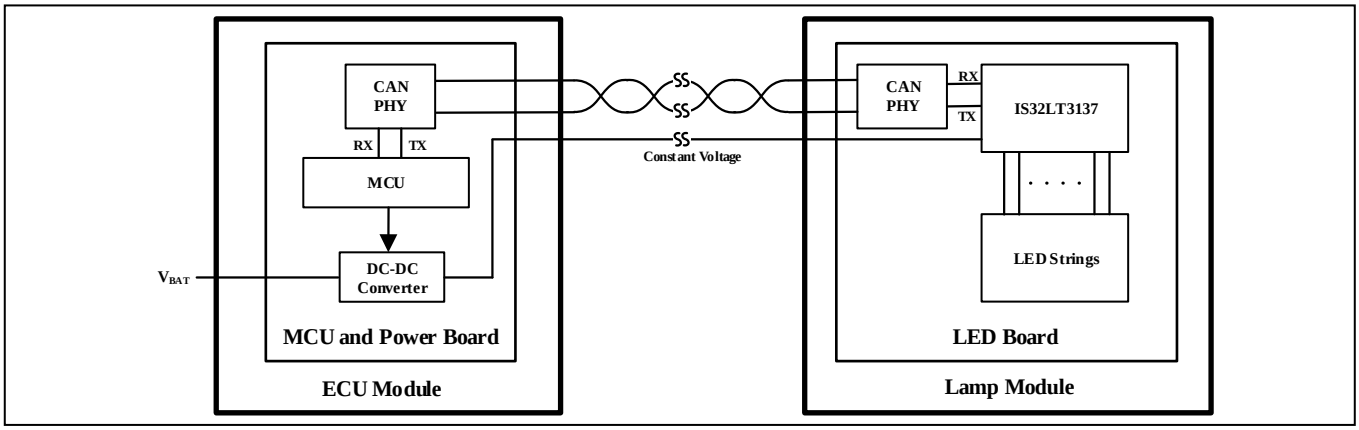


Figure 4 UART Interface with External CAN Transceiver for Outside Module Long Distance Communication

9.2 POWER SUPPLY

9.2.1 VIN UNDERVOLTAGE-LOCKOUT (UVLO)

The IS32LT3137 features an undervoltage-lockout (UVLO) function on the VIN pin to prevent unintended operation at too low supply voltages. UVLO threshold is an internally fixed value and cannot be adjusted. Entering UVLO will reset all registers to their default value. The device is disabled when the VIN voltage drops below V_{VIN_UV} and automatically resumes normal operation when the VIN voltage rises above (V_{VIN_UV}+ V_{VIN_UVHY}).

9.2.2 INTERNAL 4.2V LINEAR REGULATOR (VDD)

The IS32LT3137 device integrates an internal linear regulator (LDO) with 4.2V (Typ.) and I_{DD_MAX} current capability to provide power supply to the internal analog and digital circuits. During operation, the internal circuitry can be subject to transient currents from this linear regulator. Therefore, a 4.7μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND, it must be placed as close to the VDD pin as possible. This linear regulator also has the UVLO feature. The device is disabled when the V_{DD} voltage drops below V_{DD_UV} and resumes normal operation when the VDD voltage rises above (V_{DD_UV}). Entering UVLO will reset all registers to their default value. An I_{DD_LIM} current limit on VDD pin protects the IS32LT3137 from VDD output overload or short-circuit conditions.

9.2.3 VIO VOLTAGE SUPPLY

The positive voltage rail of the UART interface is supplied with the VIO pin which must be connected to a proper voltage source. Usually, the VIO pin should be connected to the same power supply as the MCU. If a 5V MCU is used for IS32LT3137 control, the VIO pin can be directly connected to the VDD pin.

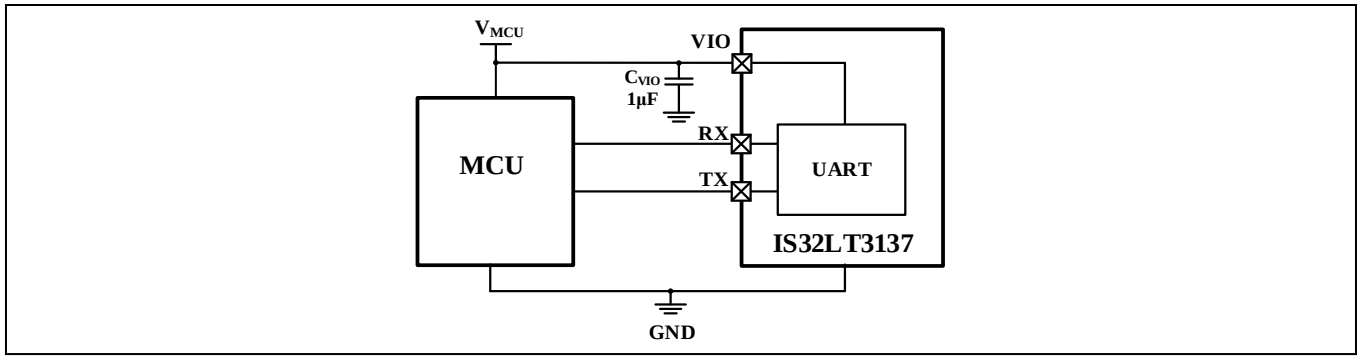


Figure 5 VIO Voltage Supply

9.3 OUTPUT CURRENT SETTING

The full DC output current (I_{OUT_FU}) for each channel is set with resistor (R_{ISET}) connected from the ISET pin to GND. This current set resistor is computed using the following equation:

If the CM bit in the CONFIG register (00h) is set to "0":

$$I_{OUT\_FU} = \frac{V_{ISET}}{R_{ISET}} \times 500 \qquad (1)$$

Where V_{ISET} is the voltage of ISET pin, when V_{ADJ} is lower than 2V (Typ.),

$$I_{OUT\_FU} = \frac{V_{ADJ}}{R_{ISET}} \times 500 \qquad (2)$$

(10kΩ ≤ R_{ISET} ≤ 75kΩ)

If the CM bit in the CONFIG register (00h) is set to "1":

$$I_{OUT\_FU} = \frac{V_{ISET}}{R_{ISET}} \times 165 \qquad (3)$$

Where V_{ISET} is the voltaeg of ISET pin, when V_{ADJ} is lower than 2V (Typ.),

$$I_{OUT\_FU} = \frac{V_{ADJ}}{R_{ISET}} \times 165 \qquad (4)$$

(10kΩ ≤ R_{ISET} ≤ 75kΩ)

It is recommended that R_{ISET} be a 1% accuracy resistor with good temperature characteristic to ensure stable output current. R_{ISET} must be placed as close to ISET pin as possible on PCB layout to avoid noise interference and ground bounce. The device is protected from an output overcurrent condition caused by R_{ISET} resistor. The output current is reduced to 17mA (Typ.) if the ISET pin is shorted to ground or R_{ISET} resistor value is too low.

When R_{ISET} is fixed, the DC output current for each channel can be further adjusted in 64-steps by the GCC[5:0] bits in the GC_CTRL register (01h). Furthermore, based on the GCC[5:0] setting, each channel also supports individual 128-step programmable DC output current adjustment. This feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on an external visual calibration system to further save binning cost. The 7-bit Scaling Registers SCAx (14h~1Fh) individually set the DC output current of each channel.

GCC[5:0] and SCAx control the OUTx current (I_{OUTx}) as shown in following equation:

$$I_{OUTx} = I_{OUT\_FU} \times \frac{GCC}{64} \times \frac{SCAx}{128} \qquad (5)$$

Where, x is from 1 to 12 for different output channel.

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \qquad (6)$$

$$SCAx = \sum_{n=0}^{6} D[n] \cdot 2^n \qquad (7)$$

For example: assume GCC[5:0] = 0x05 and SCA1 = 0x40. GCC = 5. Then the DC output current of OUT1 is:

$$I_{OUT1} = I_{OUT\_FU} \times \frac{5}{64} \times \frac{64}{128}$$

If any channel(s) are unused, please connect the corresponding OUTx pin(s) to the GND pin to avoid false fault detection and set the corresponding PWM and scaling registers to “0x00” to turn off these output(s).

9.4 ANALOG DIMMING

The IS32LT3137 offers an analog dimming input pin, ADJR. The dimming voltage range of ADJR pin is 0.06V to 2V. The global output current can be regulated by the ADJR pin voltage. If the analog dimming pin ADJR is pulled up above 2V, analog dimming is disabled, and the output current is 100% (full current). When the ADJR pin is driven below 2V, the analog dimming is enabled, and the pin voltage (0.06~2V) will proportionally control the output current.

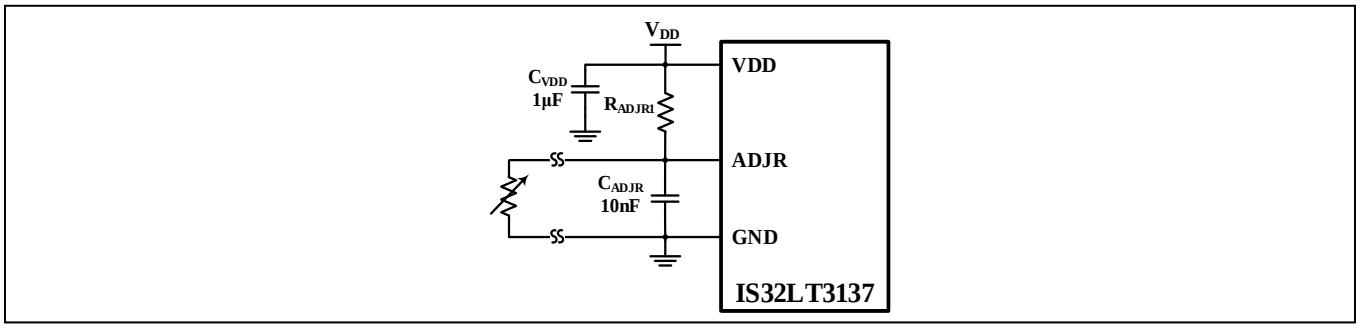


Figure 6 IS32LT3137 Analog Dimming for LED Binning

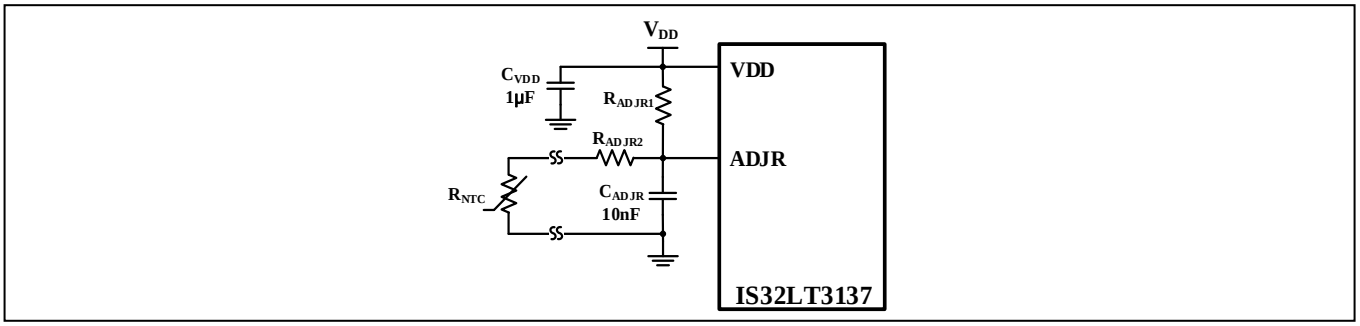


Figure 7 IS32LT3137 Analog Dimming for Thermal Roll-off

The ADJR pin can be used to fine tune the output current for LED binning during mass-production. The ADJR pin can also be used in conjunction with an NTC thermistor to provide over temperature current roll-off protection for the LED load or the system. As shown in Figure 6 and Figure 7, the IS32LT3137 can perform either LED binning or thermal roll-off function, not both at the same time.

9.5 PWM DIMMING

The IS32LT3137 integrates independent 12-bit PWM generators for each output channel. The output current for each channel is turned on and off as controlled by the PWM generator. The average current of each output channel can be adjusted by it’s PWM duty cycle to control the LED channel brightness. The PWM Registers (26h~36h) individually set the PWM duty cycle for each channel.

The PWM dimming frequency is programmable by the CONFIG register (00h). The maximum PWM frequency can be up to 24kHz (Typ.). Due to the output current slew rate control, a high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio. At a 100Hz~500Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower. Select the PWM dimming frequency based on the minimum brightness requirement for the application.

The PWM generators dim the LEDs by its duty cycle:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (8)$$

Where, D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (26h~40h), in 12bit or 7+5-bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{11} D[n] \cdot 2^n}{4096} \qquad (9)$$

In 8bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=4}^{11} D[n] \cdot 2^n}{256} \qquad (10)$$

9.5.1 PWM SPREAD SPECTRUM

The IS32LT3137 includes a spread spectrum feature on PWM base clock to optimize EMI performance. The spread spectrum function helps spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. With spread spectrum, the EMI test can be passed with smaller size and lower cost filter circuit. Spread spectrum is enabled/disabled by the SSCCFG register (4Ah).

9.5.2 PWM PHASE DELAY

To mitigate transient current generation and power supply ripple, the IS32LT3137 features PWM phase delay. When PWM phase delay is disabled (PHASE_CTRL(03h) is set to “0x00”, default value is 0x01 phase delay enable), all channels are simultaneously turned on at the beginning of each PWM cycle. This will result in large current draw from power supply leading to high voltage ripple on the power supply rail. As shown in figure 8.

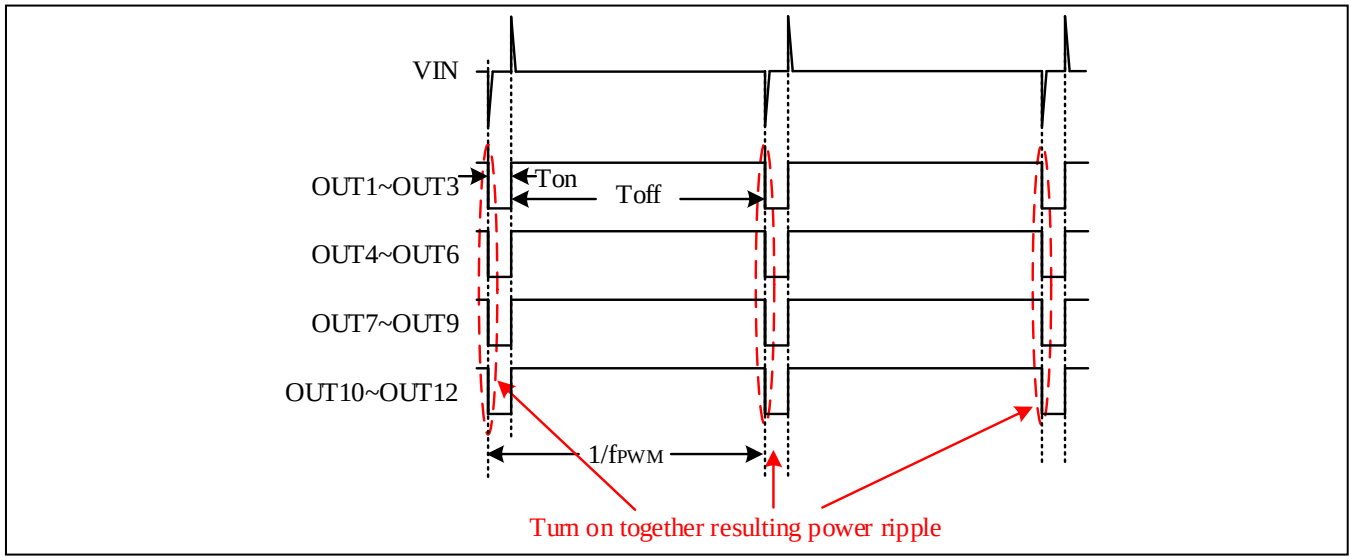


Figure 8 PWM Phase Delay Disabled

The IS32LT3137 divides 12 output channels into 4 groups to perform PWM phase delay, OUT1&OUT2&OUT3 as group 1, OUT4&OUT5&OUT6 as group 2, …OUT10&OUT11&OUT12 as group 4. When the PDE bit in the PHASE_CTRL register (03h) is set to "1", the phase delay is enabled, starting each group in turn from each PWM cycle. The t_{DELAY_1} is interval delay time between group 1 & group 2, group 3 & group 4, and t_{DELAY_1} is 1/8 PWM cycle ($1/f_{PWM}$). The t_{DELAY_2} is interval delay time between group 2 & group 3, and t_{DELAY_2} is 1/4 PWM cycle ($1/f_{PWM}$). This minimizes the voltage ripple on the VIN power supply rail. As shown in figure 9.

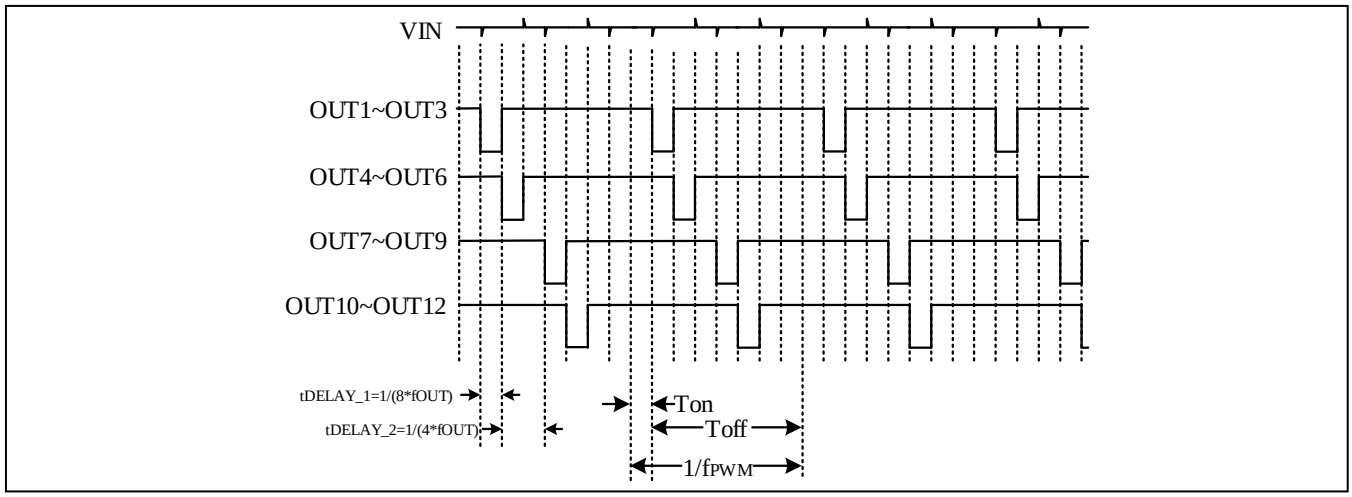


Figure 9 PWM Phase Delay Enabled

9.6 FAULT PROTECTION

9.6.1 FAULT REPORTING

For added system reliability, the IS32LT3137 integrates various fault detections for LED string open/short, single LED short, overcurrent (ISET shorted), over temperature, CRC error and watchdog timeout (fail-safe modes) conditions. The open drain pin FAULTB can be used for fault condition reporting. If any fault occurs, the corresponding bit in FLT_TYPE register will be set to “1” and the FAULTB pin will go low after a delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report fault condition. When it’s monitored by a host MCU, a pull-up resistor R_{FPU} (10kΩ recommended) from the FAULTB pin to the supply of the host MCU is required.

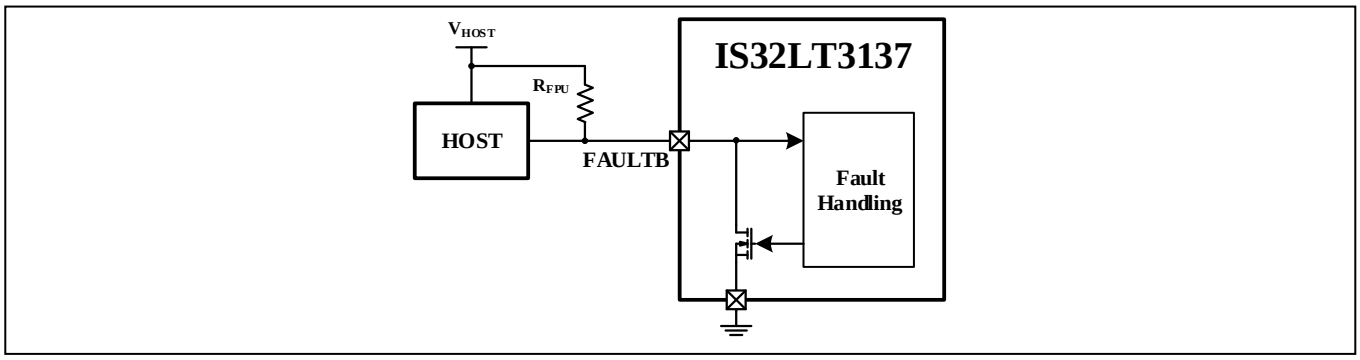


Figure 10 Host Monitors the Fault Reporting

9.6.2 LED STRING OPEN PROTECTION

The LED string open detection is enabled by setting the ODE and ODF bits in FLT_DET_EN register (4Ch) to “1”. If any LED string is opened, the corresponding OUTx pin voltage will be pulled down close to zero. When the OUTx pin voltage, V_{OUTx}, falls below the LED string open detection voltage, V_{OC_FL} and persists for longer than a deglitch time (typical 10μs), the LED string open protection will be triggered. The corresponding fault flag bits in OPEN_FLT register (51h & 52h) and the OPENF bit in FAULT_TYPE register (57h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device will recover to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) expires once the open condition is removed, i.e. V_{OUTx} rising above the LED string open detection voltage, V_{OC_RS}. The corresponding fault flag bit in OPEN_FLT register will reset to “0”. However, the OPENF bit in FAULT_TYPE register (57h) is latched, which means that it cannot automatically reset to “0” after open condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string open detection is only enabled during the PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string open fault.

9.6.3 LED STRING SHORT PROTECTION

The LED string short detection is enabled by setting the SDE and SDF bits in FLT_DET_EN register (4Ch) to “1”. If any LED string is short, the corresponding OUTx pin will be pulled up close to V_{IN}. When dropout voltage from the VIN pin to the OUTx pin, V_{IN}-V_{OUTx} (when SHORT_FLT(4Bh) = “000”), rises above the LED string short detection voltage, V_{SC_RS}, and persists for longer than a deglitch time (typical 10μs), the LED string short protection will be triggered. The corresponding fault flag bits in SHORT_FLT register (4Eh & 4Fh) and the SHORTF bit in FAULT_TYPE register (57h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the short condition is removed, V_{OUTx} falling above the LED string short detection voltage, V_{SC_FL}. The corresponding fault flag bit in SHORT_FLT register will reset to “0”. However, the SHORTF bit in FAULT_TYPE register (57h) is latched, which means that it cannot automatically reset to “0” after short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string short fault.

When the device is operated in DC mode, the PWM function is disabled. It is recommended to not enable both LED string short and single LED short, because the IS32LT3137 may incorrectly report an LED string short as a single LED short. Individually enable either LED string short or single LED short detection. If a single LED short is reported, double check for LED string short or single LED short in software.

9.6.4 SINGLE LED SHORT PROTECTION

The single LED short detection is enabled by setting the SLSDE and SLSDF bits in FLT_DET_EN register (4Ch) to "1". Then the single LED short detection is active after VIN voltage rising above the fault undervoltage-lockout voltage threshold V_{FLT_UV}. That helps to prevent false fault detection due to the insufficient power supply voltage, such as power up transience. The single LED short detect threshold V_{SLSTH} of each channel is individually programmed by the corresponding LEDx_SLS[4:0] bits in LEDx_SLSTH registers (41h~46h). If single LED of any string is shorted, the corresponding OUTx pin voltage will rise. When the OUTx pin voltage, V_{OUTx}, rise above single LED short detect threshold, V_{SLSTH}, and persists for longer than a deglitch time (typical 10μs), the single LED short protection will be triggered. The corresponding fault flag bits in SLS_FLT register (54h & 55h & 56h) and the SLS_FLT bit in FAULT_TYPE register (57h) will be set to "1". The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

The device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the single LED short condition is removed, V_{OUTx} rising above the LED string short detection voltage, V_{SLSTH}. The corresponding fault flag bit in SLS_FLT register will reset to "0". However, the SLSHORTF bit in FAULT_TYPE register (57h) is latched, which means that it cannot automatically reset to "0" after single LED short condition being removed but must be cleared by the host MCU writing it back to "0".

When PWM dimming is implemented, the single LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any single LED short fault.

9.6.5 OUTPUT OVERCURRENT (ISET PIN SHORT)

The device is protected from an output overcurrent condition caused by the R_{ISET} resistor. All output current is limited to 110mA (Typ.) in case of the ISET pin shorted to ground or too low value R_{ISET} resistor is connected to ISET pin. If the condition persists for longer than a deglitch time (typical 1μs), the ISET pin short protection will be triggered. All output current will be reduced to 17mA (Typ.). The RSET_SH bit in FAULT_TYPE register (57h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the RSET_SH bit in FAULT_TYP register (57h) is latched, which means that it cannot automatically reset to "0" after ISET short condition being removed but must be cleared by the host MCU writing it back to "0".

9.6.6 THERMAL SHUTDOWN

If the junction temperature exceeds T_{SD} (Typ. 168˚C), all output channels will go to the OFF state and the TSD bit in FAULT_TYPE register (57h) will be set to "1". If the TRE bit in TEMP_SEN register (02h) to "1", the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. At this point, the device presumably begins to cool off. Any attempt to toggle the channels back to the source condition before the device has cooled to below (T_{SD}-T_{SD_HYS}) (Typ. 155˚C) will be blocked and the device will not be allowed to restart. The FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the device cools down. However, the TSD bit in FAULT_TYPE register (57h) is latched, which means that it cannot automatically reset to "0" but must be cleared by the host MCU writing it back to "0".

9.6.7 THERMAL ROLL-OFF PROTECTION

The device integrates the thermal shutdown protection to prevent the device from overheating. In addition, to prevent the LEDs from flickering due to rapid thermal changes, the device also includes a programmable thermal roll-off feature to reduce power dissipation at high junction temperature.

The output current will be equal to the set value I_{OUTx} if the junction temperature of the device remains below thermal roll-off temperature threshold 140˚C. If the junction temperature exceeds the temperature threshold, the output current of all channels will begin to linearly reduce following the junction temperature ramping up until thermal

shutdown. The TF bit in FAULT_TYPE register (57h) will be set to “1”. If the TRRE bit in TEMP_SEN register (02h) to “1”, the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The percentage of the output current before thermal shutdown is programmable by the TROF[2:0] bits in the TEMP_SEN register (02h).

The output current will linearly resume to the set value I_{OUTx} and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the junction temperature cools down below the thermal roll-off temperature threshold 140˚C. However, the TF bit in FAULT_TYPE register (57h) is latched, which means that it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

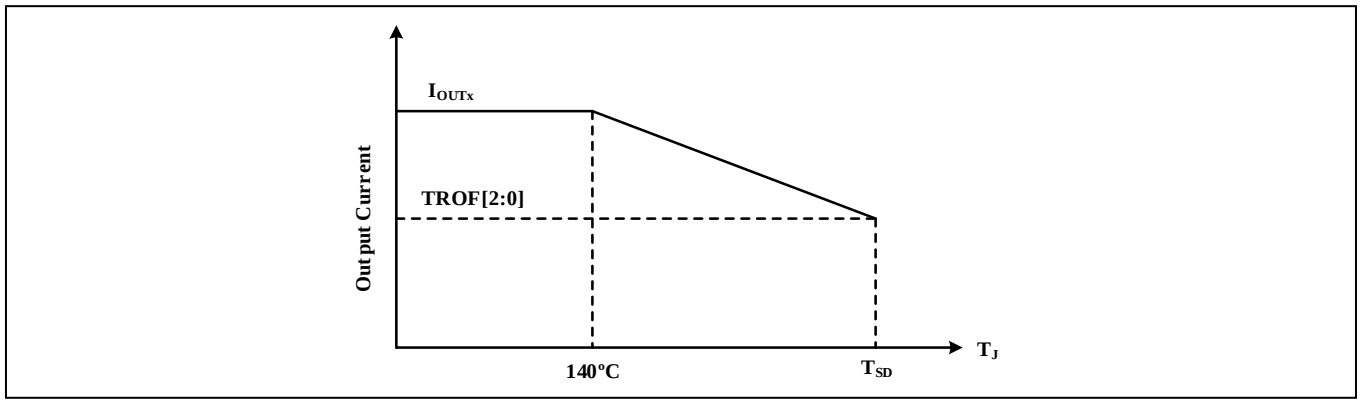


Figure 11 Thermal Roll-off Protection

By mounting the IS32LT3137 device on the same thermal substrate as the LEDs, use of this feature can also limit the dissipation of the LEDs.

Fault Action Table (Both Normal State And Fail-Safe State)

Fault Type	Detection	Conditions	Actions	Fault Flags	FAULTB Pin	Recovery
Supply UVLO	$V_{IN}<V_{VIN\_UV}$ or $V_{DD}<V_{DD\_UV}$	-	Turn off all channels and reset all registers to default value	-	No action	$V_{IN}>(V_{VIN\_UV}+V_{VIN\_UVHY})$ or $V_{DD}>(V_{DD\_UV}+V_{DD\_UVHY})$
LED string open	$V_{IN}>V_{FLT\_UV}$ and $V_{OUTx}<V_{OC\_FL}$	PWM pulse width greater than 10μs (Typ.) and ODE = 1, ODF = 1	Faulty channel outputs 4mA and other channels on (ODF = 1)	OPEN_FLT and OPENF bit	Pull low	$V_{OUTx}>V_{OC\_RS}$ Write OPENF bit to “0”
LED string short	$(V_{IN} - V_{OUTx}) <V_{SC\_RS}$ (SHORT_FLT=000) or $V_{OUTX} > V_{SC}$ (SHORT_FLT≠000)	PWM pulse width greater than 10μs (Typ.) and SDE = 1, SDF = 1	Faulty channel outputs 4mA and other channels on (SDF = 1)	SHORT_FLT and SHORTF bit	Pull low	$(V_{IN} - V_{OUTx}) >V_{SC\_FL}$ (SHORT_FLT=000) or $V_{OUTX} < V_{SC}$ (SHORT_FLT≠000) Write SHORTF bit to “0”
Single LED short	$V_{IN}>V_{FLT\_UV}$ and $V_{OUTx}>V_{SLSTH}$	PWM pulse width greater than 10μs (Typ.) and SLSDE = 1, SLSDF = 1	Faulty channel outputs 4mA and other channels on (SLSDF = 1)	SLST_FLT and SLSHORTF bit	Pull low	$V_{OUTx}<V_{SLSTH}$ Write SLSHORTF bit to “0”
ISET pin short (Overcurrent)	I_{OUTx} limited to 110mA (Typ.)	Longer than 1μs (Typ.) deglitch time	All channels reduced to 17mA (Typ.)	RSET_SH bit	Pull low	ISET pin to GND resistance resumes to normal range, Write RSET_SH bit to “0”
Thermal shutdown	$T_J>T_{SD}$	-	All channels off	TSD bit	Pull low (TRE = 1)	$T_J<(T_{SD}-T_{SD\_HYS})$ Write TSD bit to “0”
Thermal roll-off	$T_J>140^{\circ}C$	TROF[2:0] ≠ 00	All channels linearly reduce output current	TF bit	Pull low (TRRE = 1)	$T_J<140℃$ Write TF bit to “0”
CRC error	Calculated CRC does not match CRC data	-	Increments CRC Error Count register	CRCF bit	Pull low	Write CRCF bit to “0”
Communication loss	Watchdog times out	R_{FSMD}=30kΩ, 51kΩ or 75kΩ and no error-free communication	Enter fail-safe modes	CMWF bit	Pull low	Write CMWF bit to “0”

Note 8: OPENF, SHORTF, SLSHORTF, ISETSF, TSD, TF, CMWF and CRCF bits are latched. Even though the fault conditions are removed, they cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

9.7 UART INTERFACES

The host MCU can communicate with the IS32LT3137 device using a Universal Asynchronous Receiver and Transmitter (UART). The UART communication process uses a command and response protocol mastered by the host MCU to write and read the registers to and from each IS32LT3137 device. The IS32LT3137 UART interface utilizes half-duplex communications (transmit and receive cannot overlap). A tri-state buffer in the IS32LT3137 drives the TX out pin, so it is recommended to place an external pull-up resistor on the RX input return line of the host MCU. An external pull-up on the MCU TX output will allow multiple IS32LT3137 devices to share a common pair of TX and RX signals by connecting all IS32LT3137 TX lines together and all IS32LT3137 RX lines together. The baud rate can support 100kbps~1Mbps.

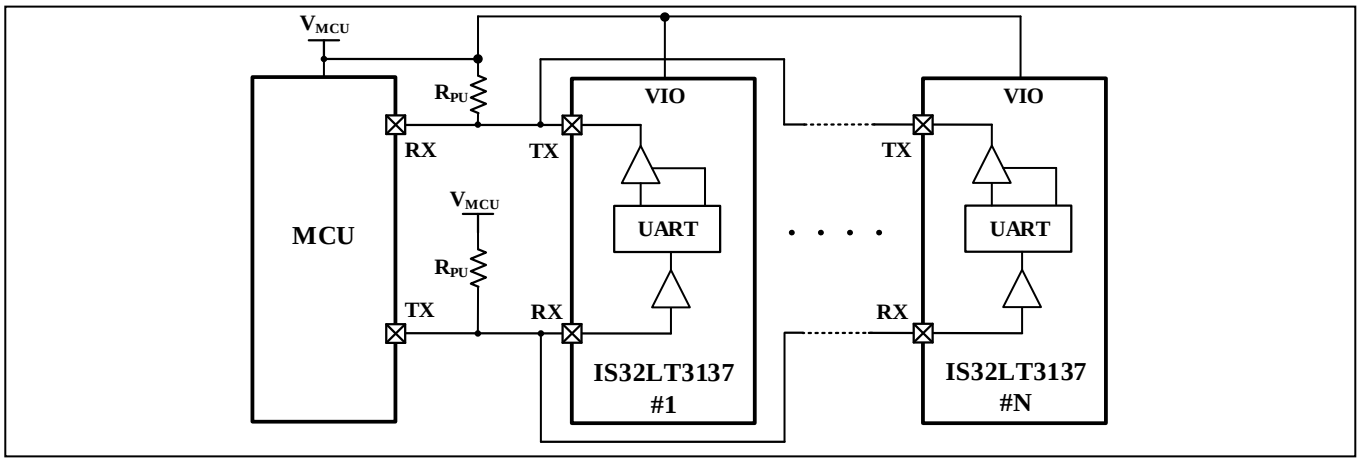


Figure 12 UART Interface Connection

Additionally, the physical TX and RX connections of IS32LT3137 can be joined together through a standard CAN transceiver (CAN PHY), as shown in Figure 13. This has the added advantage of protection from shorts to battery and/or shorts to ground on the cables and/or harnesses between the host MCU board and the IS32LT3137 board. The CAN physical layer has excellent EMI and EMS performance with long distance off-board connection.

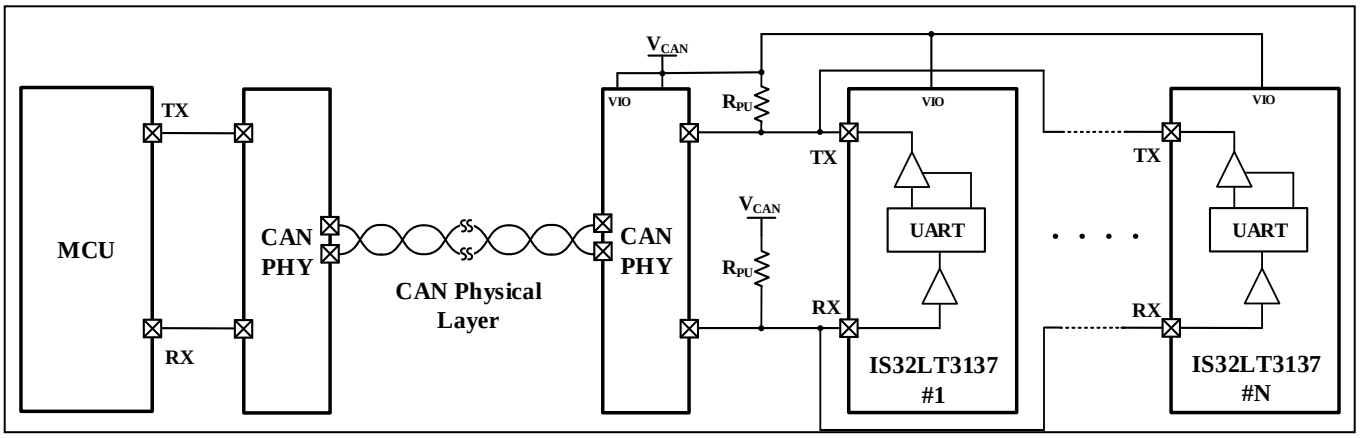


Figure 13 UART Interface with Standard CAN Transceiver Connection

9.7.1 UART DATA FORMAT

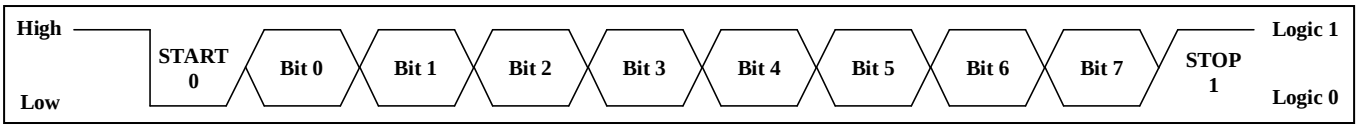


Figure 14 UART Data Byte Format

The UART operates with one start bit, eight data bits (LS bit first) and one stop bit. Above figure shows the waveform for an individual byte transfer on the UART. A logic “1” state occurs when the device drives the line to high voltage. A logic “0” state occurs when the device drives the line to ground. Below figure shows actual data bytes with UART data format.

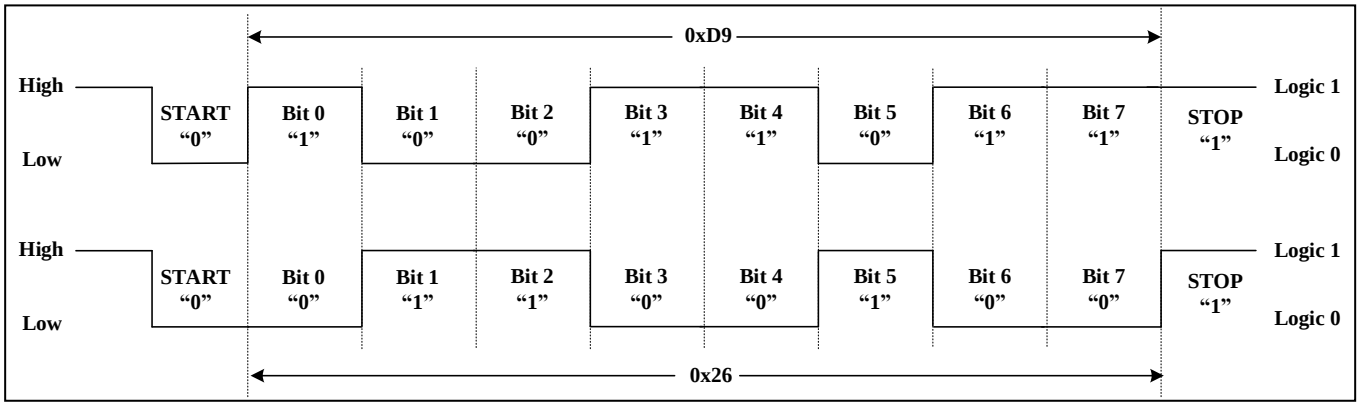


Figure 15 UART Data Transaction Example

The baud rate of UART communication can be 100kbps to 1Mbps which is synchronized by the baud rate of the SYNC byte of the BUS Reset command. The UART uses 32x over-sampling on the incoming asynchronous RX signal. Between UART data bytes, at least one bit is required as STOP bit.

9.7.2 COMMUNICATION PROTOCOL

The communication process of all three interfaces uses a command and response protocol mastered by the host MCU to write and read the registers to and from each IS32LT3137 device. This means that the IS32LT3137 device never initiates traffic onto the network. The protocol maps the registers into an address space on each device. The host MCU uses the protocol to initiate a communication transaction by sending a command frame. This command frame addresses either one IS32LT3137 device directly or broadcasts to all IS32LT3137 devices on the network. This addressing may cause a response frame to be sent back from the slave IS32LT3137 device depending on the command type of the command frame. There are four types of commands:

1) BUS Reset Command: resets the UART
2) Write Command: writes data from host MCU to specific IS32LT3137 device(s)
3) Read Command: reads data from specific IS32LT3137 device to host MCU
4) Special Command: specifies IS32LT3137 device(s) to implement specific function.

There is no response frame given following a broadcast write command frame. Therefore, only two types of response frames exist that an IS32LT3137 device sends back to the host MCU: Write Acknowledge (if enabled) and Read Response.

9.7.3 COMMAND FRAME TYPES

9.7.3.1 BUS Reset Command Frame

The host MCU can reset the device UART and protocol state machine at any time by sending BUS Reset command. The BUS Reset command consists of reset signal and SYNC byte (0x55). The reset signal includes at 150μs~10ms break low and at 2μs~100us logic high break delimiter. Upon receiving the bus reset signal, the state machine of all IS32LT3137 devices on the bus will be reset to a known-good state. The bus reset signal must be followed by a SYNC byte (0x55) send by desired baud rate (within 100kbps to 1Mbps) to synchronize the baud rate to all IS32LT3137 devices. The subsequent communication must use the identical baud rate. With this synchronization approach, the cost of an external crystal oscillator is saved. To avoid clock drift over time and ambient temperature, it's recommended to periodically send a BUS Reset Command to the IS32LT3137 devices.

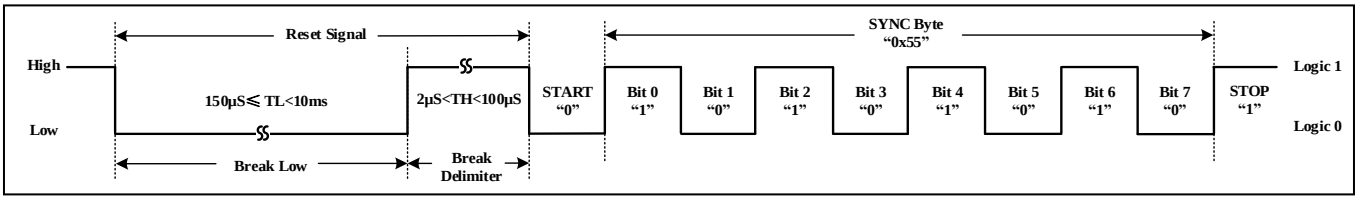


Figure 16 BUS Reset Command

Upon system power up, the host MCU must initialize the BUS by sending a BUS Reset Command before communication. This BUS reset operation can be optionally performed by the host MCU for several application scenarios: (1) upon system power up, (2) communication watchdog times out, (3) communication fault is detected, illustrated as in the following diagram:

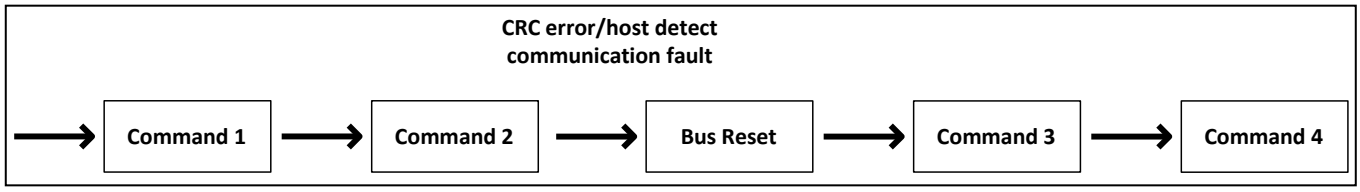


Figure 17 Communication Fault is Detected

Note that the BUS Reset command only resets the interface state machine (including stored communication baud rate). It does not reset the registers and does not halt normal LED PWM operation.

Note 9: If TX or RX anyone disconnect, there will cause CRC error, communication again need send Bus reset.

9.7.3.2 Write Command Frame

The Write Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

9.7.3.3 Acknowledge Frame

If the ACKEN bit is set in the SYSCFG register, the addressed device transmits an acknowledge back to the host MCU upon a successful single device write. The Acknowledge Frame is comprised of a single byte (ACK=0x7F) as the following sequence.

ACK (0x7F)

9.7.3.4 Read Command Frame (transferred by the host MCU)

The Read Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

A successfully-addressed IS32LT3137 device then transfers back the appropriate Read Response Frame.

The Read Response Frame is comprised of the following sequence.

RSP Frame Header (One Byte)	Device ID (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

9.7.3.5 Special Command Frame

The special command specifies the IS32LT3137 device to implement specific function which includes:

a) Update Command

This special command is used for below scenarios:

- Update the configuration of the PWM registers data and Scaling registers data into output stages at the next PWM boundary after this command is issued.
- Update the configuration of the DC_PWM_SEL register (00h).
- Update the configuration of the PHASE_CTRL register (03h).

b) Registers Reset Command

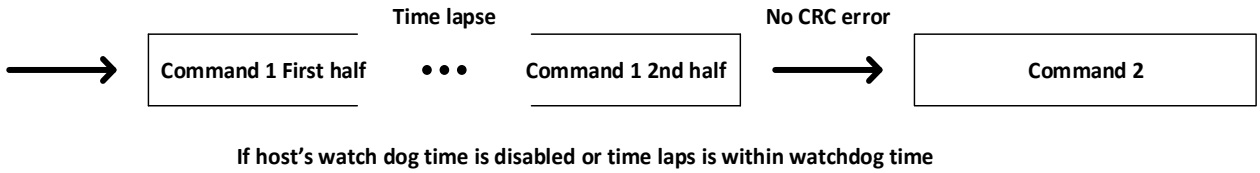
Resets all registers to default value, excluding the PWR bit in SYSCFG register (4Ah).

The Special Command Frame is comprised of the following sequence:

CMD Frame Header (One Byte)	Device ID (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

One complete command frame can be received successfully even if the bytes in the frame is not sent continuously.

CRC error could be determined by reading back the written data byte.



9.7.4 TRANSACTION FRAME DESCRIPTION

Command frames include the following byte types:

1) Frame Header Byte
2) Device ID Byte
3) Start Register Address Byte
4) N Data Byte(s) (N = 1~16, 32)
5) CRC Bytes (CRC_L and CRC_H)
6) Acknowledge Byte (ACK)

9.7.4.1 Frame Header Byte

The Frame Header Byte identifies the transaction as either a write/read command frame or a response frame. In addition, the Frame Header Byte indicates how many data bytes are being written/read or responded. The number of data bytes to be written/read or responded can be 1~16 or 32.

Frame Header Type	D7	D6	D5	D4:D0
CMD Frame Header	FRM_TYPE	W/R	BCON	CMD
RSP Frame Header	FRM_TYPE	RSVD	RSVD	RSP

The fields shown in the Frame Header Byte above are described in the table below.

	Value (BIN)	Description
FRM_TYPE (Bit 7)	0	Response frame sent back from the IS32LT3137 device to host MCU
	1	Command frame sent from host MCU to the IS32LT3137 device
W/R (Bit 6)	0	Write command frame
	1	Read command frame
BCON (Bit 5)	0	Single device write or read.
	1	Broadcast write. The Device ID Byte must be 0xBF to broadcast to all IS32LT3137 devices. Broadcast only accepts write command
CMD (Bit 4:0)	**Specify transmit data length for write/read command frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length
	For special commands (W/R bit must be set to "0"):	
	11000	Update Command. Valid for both single device and broadcast write
	11110	Registers Reset Command. Valid for both single device and broadcast write
RSP (Bit 4:0)	**Specify transmit data length for response frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length

9.7.4.2 Device ID Byte

	D7	D6	D5:D0
Device ID	p[1]	p[0]	DEV_ID [5:0]

There are six DEV_ID bits and two parity bits.
The parity bits for the Device ID byte are calculated with the equations below:

p[1] = ~(dev_id[1] ^ dev_id[3] ^ dev_id[4] ^ dev_id[5])

p[0] = dev_id[0] ^ dev_id[1] ^ dev_id[2] ^ dev_id[4]

The device ID of each IS32LT3137 device is determined by the resistors connected from three address pins of ADDR0 and ADDR1 to GND. As following mapping for the Device ID byte. For a broadcast command of UART interface, the DEV_ID[5:0] must be 0b 111111, and the pin 30 should be left floating (Note 10), otherwise the broadcast command will be invalid.

R_{AD1} (kΩ, Note 10)	R_{AD0} (kΩ, Note 10)	D7	D6	D5	D4	D3	D2	D1	D0	DEVICE ID (HEX)
10k	10k	0	0	0	0	0	0	1	1	03
10k	30k	1	1	0	1	0	0	1	1	D3
10k	51k	1	0	1	0	0	0	1	1	A3
10k	75k	0	1	1	1	0	0	1	1	73
30k	10k	0	1	0	0	0	1	1	1	47
30k	30k	1	0	0	1	0	1	1	1	97
30k	51k	1	1	1	0	0	1	1	1	E7
30k	75k	0	0	1	1	0	1	1	1	37
51k	10k	1	0	0	0	1	0	1	1	8B
51k	30k	0	1	0	1	1	0	1	1	5B
51k	51k	0	0	1	0	1	0	1	1	2B
51k	75k	1	1	1	1	1	0	1	1	FB
75k	10k	1	1	0	0	1	1	1	1	CF
75k	30k	0	0	0	1	1	1	1	1	1F
75k	51k	0	1	1	0	1	1	1	1	6F
75k	75k	1	0	1	1	1	1	1	1	BF
-	-	1	0	1	1	1	1	1	1	BF (Note 11) (for broadcast command only)

Note 10: The tolerance range of resistance accuracy could be ±1% or ±5% for 10kΩ, 30kΩ, and 75kΩ, but the tolerance range of resistance accuracy should be ±1% for 51kΩ.

Note 11: The Device ID Byte must be 0xBF to broadcast to all IS32LT3137 devices. Broadcast only accepts write command.

Note 12: The Pin 30 should not be connected to any other pins or signals, otherwise the DEVICE ID will not be detected correctly.

Note 13: After IS32LT3137 powers on, it is suggested to wait for 3ms before sending a command, as the IS32LT3137 requires 3ms to detect its Device ID upon power-up.

9.7.4.3 Start Register Address Byte

The protocol allows up to 32 successive register locations from the addressed register to be written or read by a single command frame. The Start Register Address Byte is single byte which specifies the first register being written or read. The Start Register Address byte is present in only Write and Read Command transactions, not in Read Response and Special command transactions.

9.7.4.4 N Data Byte(s)

The Frame Header Byte specifies the number of data bytes to be included in the frame.

9.7.4.5 CRC Bytes (CRC_L and CRC_H)

The host MCU sends command to IS32LT3137 using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame bytes, e.g., Frame Header Byte, Device ID Byte, Start Register Address Byte, N Data Bytes. Lower byte first followed by higher byte. The CRC Bytes allow detection of errors within the transaction frame. The device increments the CRC Error Count Register (59h) each time a CRC error occurs on an incoming command frame and the CRCF bit in FLT_TYPE register (57H) will be set to "1" and the FAULTB pin will go low to report fault condition after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRCF bit in FLT_TYPE register (57H) is latched, which means that it cannot automatically reset to "0" when no CRC error occurs but must be cleared by the host MCU writing it back to "0". Once the CRCF bit is cleared, the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRC bytes are also calculated by the addressed device during its Read Response. The CRC bytes are then appended to the end of the read data, lower byte first followed by higher byte. This allows the host MCU to check the read data coming from the IS32LT3137 device for any transmission errors. The following is a reference CRC checksum C code for a transmission to the IS32LT3137 devices.

```
Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
{
        Uint16 crc = 0;
        Uint16 I;
        while (len--)
        {
                crc ^= *buf++;
                for (I = 0; I < 8; I++){
                crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
                }
        }
        return crc;
}
```

Upon reading data from the IS32LT3137 device, the host MCU should calculate and compare the CRC to determine whether valid data was received. When IS32LT3137 sends back CRC bytes to the host MCU, the calculated CRC bytes must be bit-reversed before comparison to the received CRC bytes. The following is a reference code to perform received CRC bit reversal.

```
Uint8 reverse_byte(Uint8 byte)
{
        // First, swap the nibbles
        byte = (((byte & 0xF0) >> 4)| | ((byte & 0x0F) << 4));
        // Then, swap bit pairs
        byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
        // Finally, swap adjacent bits
        byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
        // We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
        return byte;
}
```

The following is a reference code for checking the read data against received CRC bytes.

```
bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
{
        Uint16 crc_calc; // Calculated CRC
        Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
        // Calculate the CRC based on bytes received
        crc_calc = crc_16_ibm(rx_buf, crc_start);
        crc_lsb = (crc_calc & 0x00FF);
        crc_msb = ((crc_calc >> 8) & 0x00FF);
        // Perform the bit reversal within each byte
        crc_msb = reverse_byte(crc_msb);
        crc_lsb = reverse_byte(crc_lsb);
```

```
        // Do they match?
        if((*(rx_buf + crc_start) == crc_lsb) && (*(rx_buf + crc_start + 1) == crc_msb))
        {
                return TRUE;
        }
        else
        {
                return FALSE;
        }
}
```

9.7.4.6 Acknowledge Byte

The Acknowledge Byte (“ACK”) consists of a single byte (ACK=0x7F):

ACK is sent back by the addressed IS32LT3137 device only if the ACKEN bit is set in the SYSCFG register (4Ah) and only if the write is successful. A successful write yields no CRC checksum error or parity errors. Note that the acknowledge is only valid for single device write transaction of IS32LT3137.

9.7.4.7 Turnaround Time

When considering back-to-back data transfer, the turnaround time (additional time required between the end of the previous byte stop bit and the beginning of the next byte start bit) is required, that means a finite amount of dead time must be inserted between two bytes or two command frames. It’s recommended to use dual stop bits mode for the UART interface.

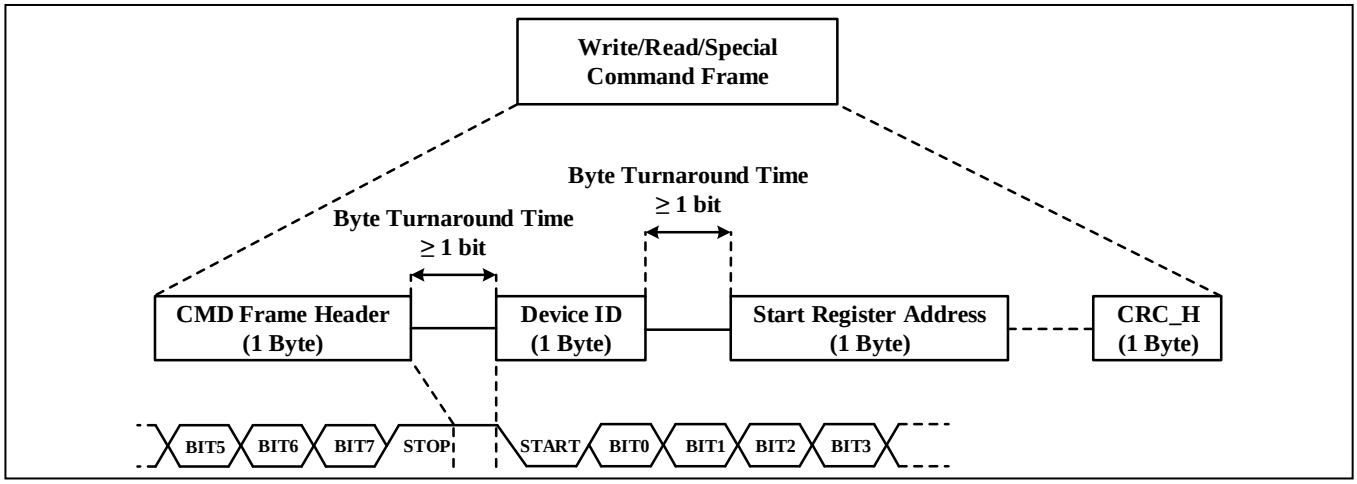


Figure 18 Turnaround Time Between Byte to Byte

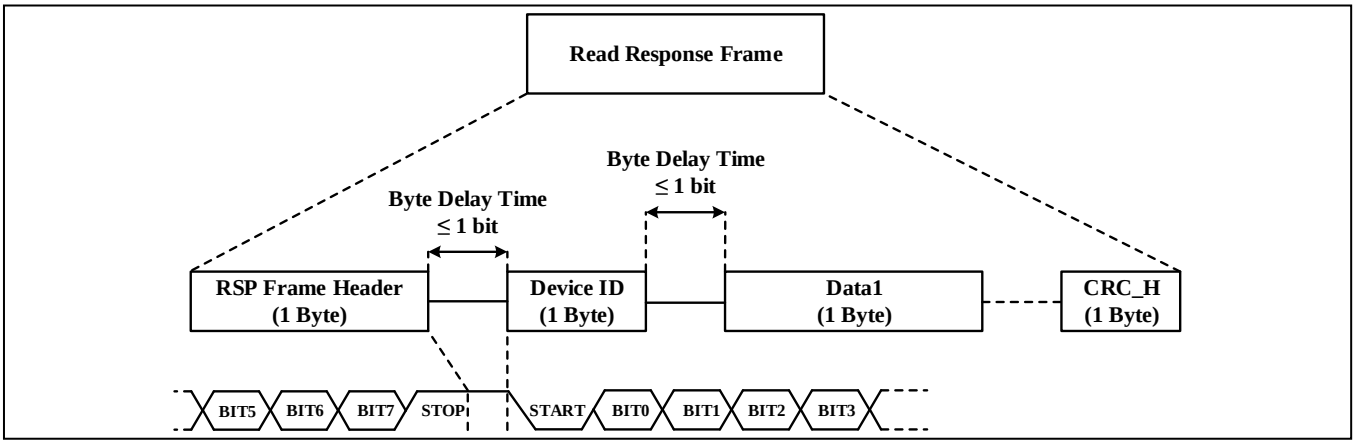


Figure 19 Delay Time Between Byte to Byte of Read Response Frame

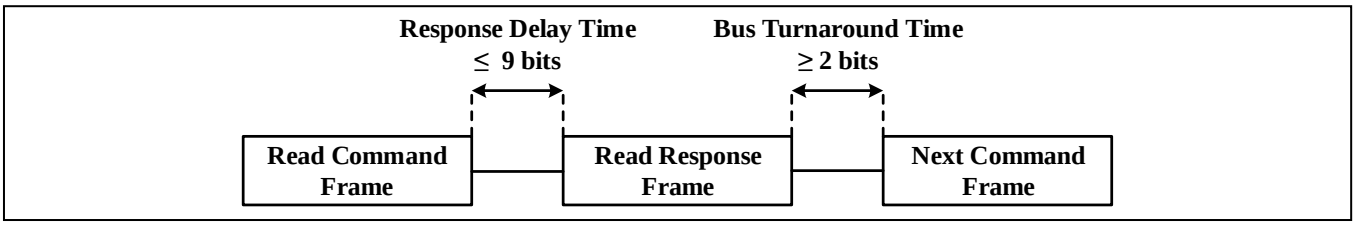


Figure 20 Turnaround Time Between Read Response Frame to Next Command Frame

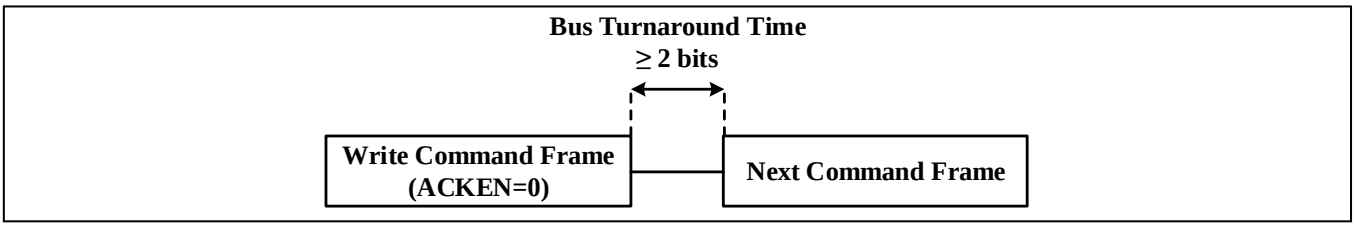


Figure 21 Turnaround Time Between Write Command Frame to Next Command Frame (ACK Disabled)

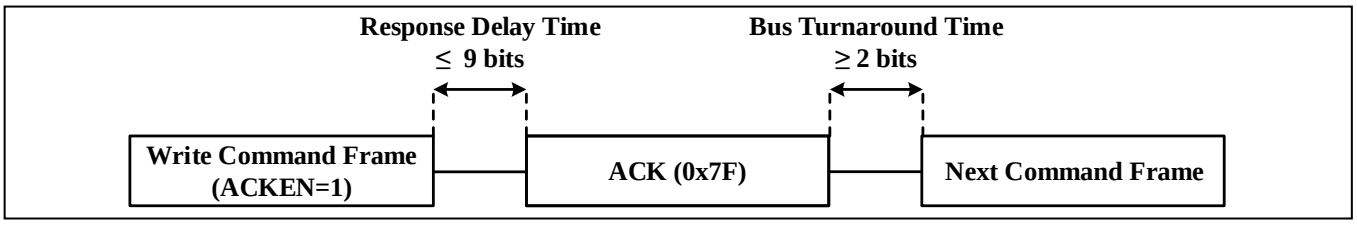


Figure 22 Turnaround Time Between ACK to Next Command Frame (ACK Enabled)

9.8 COMMUNICATIONS EXAMPLES

The total number of transmitted bytes depends on the specific task being performed. The examples below show the sequence of transmitted bytes for a given transaction.

9.8.1 Example 1: Single Device Write of 3 Bytes

Write to Device ID with parity = 0xE7, R_{AD0}=51kΩ, R_{AD1}=30kΩ: beginning at register 26h, PWM1_H=0x1F, PWM2_H=0x2F, PWM1_2_L=0x3F

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

	Command Frame							
Interface	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART	0x82 (0b10000010)	0xE7	0x26	0x1F	0x2F	0x3F	0x4C	0x9A

Acknowledge from addressed device (if enabled ACKEN bit for IS32LT3137)

Acknowledge Frame
ACK
0x7F

9.8.2 Example 2: Single Device Read of 2 Bytes

Read from Device ID with parity = 0xA3, R_{AD0}=51kΩ, R_{AD1}=10kΩ: beginning at register 57H, read FLT_TYPE

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
CRC Bytes	2
Total	5

	Command Frame				
Interface	**CMD Frame Header**	**Device ID**	**Start Register Address**	**CRC_L**	**CRC_H**
UART	0xC1 (0b11000001)	0xA3	0x57	0x39	0x32

Read Response: FLT_TYPE=0x00

Byte Types	Number of Bytes
RSP Frame Header Byte	1
Device ID Byte	1
Data Bytes	2
CRC Bytes	2
Total	6

	Command Frame					
Interface	**RSP Frame Header**	**Device ID**	**Data 1**	**Data 2**	**CRC_L**	**CRC_H**
UART	0x01 (0b00000001)	0XA3	0x00	0x00	0x8F	0x7B

9.8.3 Example 3: Broadcast Write of 3 Bytes

Broadcast write to all devices (fixed Device ID with parity = 0xBF): beginning at register 14h, SCA1=0x0F, SCA2=0x1F, SCA3=0x2F

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

	Command Frame							
Interface	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART	0xA2 (0b10100010)	0xBF	0x14	0x0F	0x1F	0x2F	0x70	0x86

9.8.4 Example 4: Broadcast Registers Reset Command (Special Command)

Broadcast Registers Reset Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	CMD Frame Header	Device ID	CRC_L	CRC_H
UART	0xBE (0b10111110)	0xBF	0x30	0x10

9.8.5 Example 5: Broadcast Update Command (Special Command)

Broadcast Update Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	CMD Frame Header	Device ID	CRC_L	CRC_H
UART	0xB8 (0b10111000)	0xBF	0x33	0xB0

9.9 DEVICE FUNCTIONAL MODES

The IS32LT3137 device operates in one of several states.

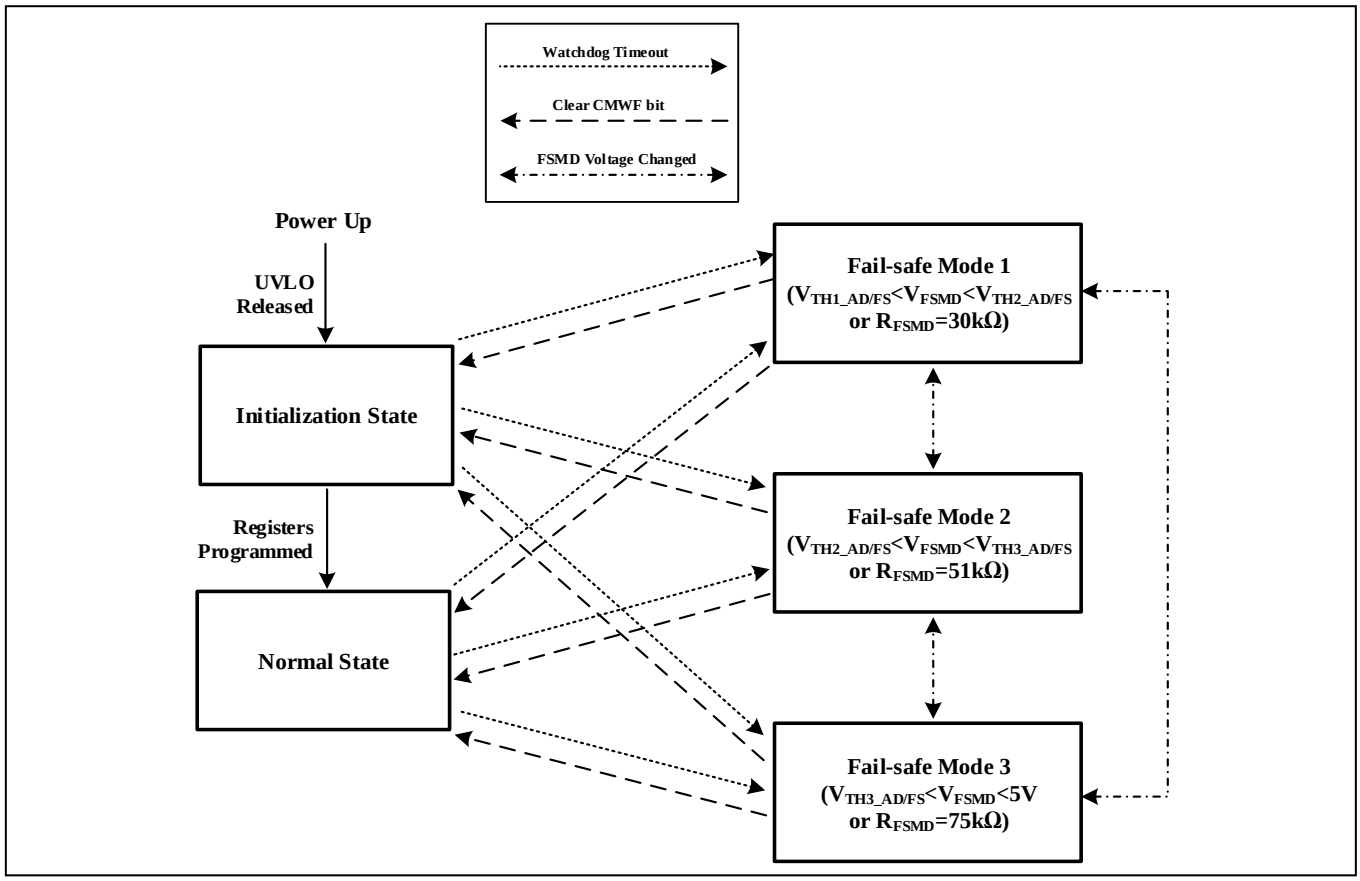


Figure 23 Operation States

9.9.1 INITIALIZATION STATE

On power up and once released from UVLO, the device enters an initialization state. In this state, all registers are reset to default values and all outputs are in off state. The device waits to receive commands from the MCU master.

9.9.2 NORMAL STATE

In normal state, the IS32LT3137 registers control its outputs by accepting interface commands and by monitoring and responding to realtime events on the inputs associated with the analog and power circuitry. This allows dimming of the LED outputs using the registers settings.

9.9.3 FAIL-SAFE STATE

This state allows the user to preset the outputs' state if the communication is broken. The device integrates a communication watchdog timer that operates based on the system clock pulse. The tap point, programmed via CMWTAP register (4Ah), defines the timing of the communication watchdog timer (a 24-bit/25-bit counter). By default, the tap point is set to bit 22, which means the device requires 2^22 (or 2^21) system clock cycles for the communication watchdog timer to time out. If the communication watchdog times out (no error-free communication is successfully received for the programmed number of system clock cycles), the device will enter fail-safe mode which includes three modes, Mode 1 ~ Mode 3.

The FSMD pin is used to configure the fail-safe modes. When the resistor R_{FSMD} is connected from the FSMD pin to ground, the internal $I_{AD/FS}$ (typical 50μA) current source creates a voltage on the FSMD pin, V_{FSMD}. The device compares the V_{FSMD} with internal different reference voltage levels ($V_{TH1\_AD/FS}$, $V_{TH2\_AD/FS}$ and $V_{TH3\_AD/FS}$) to determine the fail-safe mode. It also allows to externally apply proper voltage on the FSMD pin to either choose or change the fail-safe mode. Refer to the Fail-safe Mode Setting Table.

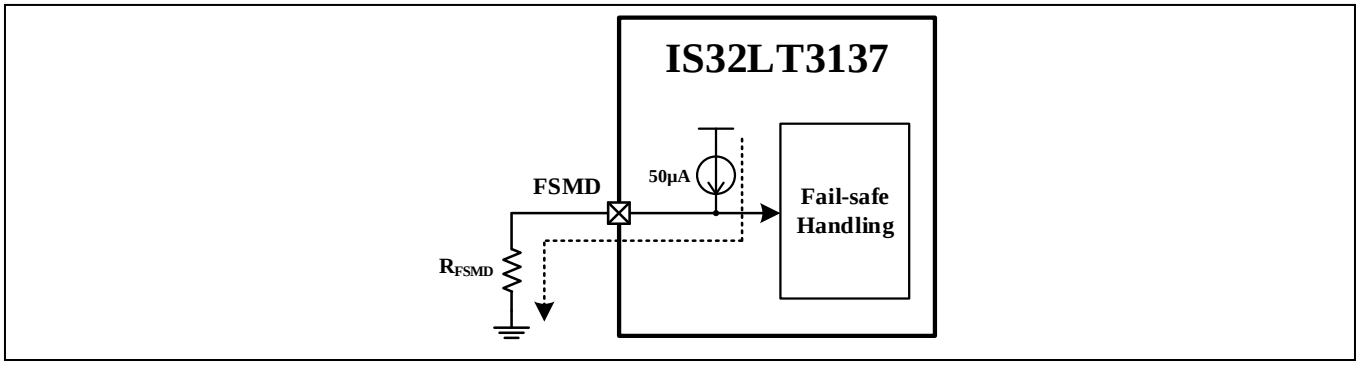


Figure 24 Fail-safe Mode Setting

When 0V<V_{FSMD}<$V_{TH1\_AD/FS}$, or R_{FSMD}=10kΩ, the internal communication watchdog is invalid, and the fail-safe mode is disabled. The outputs are always controlled by the scaling and PWM registers (14h~36h).

When $V_{TH1\_AD/FS}$<V_{FSMD}<$V_{TH2\_AD/FS}$, or R_{FSMD}=30kΩ, the internal communication watchdog is active, and the fail-safe mode is Mode 1. If the watchdog times out, the device will enter fail-safe Mode 1 and the outputs will be determined by the DEFAULT registers (07h~10h). The CMWF bit in FLT_TYPE register (57H) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF bit in FLT_TYPE register (57H) must be cleared by the host MCU writing it to "0". The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH2\_AD/FS}$<V_{FSMD}<$V_{TH3\_AD/FS}$, or R_{FSMD}=51kΩ, the internal communication watchdog is active, and the fail-safe mode is Mode 2. If the watchdog times out, the device will enter fail-safe Mode 2 and all outputs will be forced into completely off. The CMWF bit in FLT_TYPE register (57H) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF bit in FLT_TYPE register (57H) must be cleared by the host MCU writing it to "0". The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH3\_AD/FS}$<V_{FSMD}<5V, or R_{FSMD}=75kΩ, the internal communication watchdog is active, and the fail-safe mode is Mode 3. If the watchdog times out, the device will enter fail-safe Mode 3 and all outputs will be forced into fully on (with 98% PWM duty cycle). The CMWF bit in FLT_TYPE register (57H) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF bit in FLT_TYPE register (57H) must be cleared by the host MCU writing it to "0". The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

In the fail-safe modes, the fault protections also are valid, including LED string open/short, single LED short, overcurrent (ISET shorted), and over temperature.

Note that the device must be re-initialized after quitting from the fail-safe mode to normal state.

9.9.4 Fail-safe Mode Setting Table:

FSMD Pin	Fail-Safe Mode	LED State In Fail-Safe Mode
0V<V_{FSMD}<$V_{TH1\_AD/FS}$ or R_{FSMD}=10kΩ	Disabled	-
$V_{TH1\_AD/FS}$<V_{FSMD}<$V_{TH2\_AD/FS}$ or R_{FSMD}=30kΩ	Mode 1	Determined by Default Registers (07h~10h)
$V_{TH2\_AD/FS}$<V_{FSMD}<$V_{TH3\_AD/FS}$ or R_{FSMD}=51kΩ	Mode 2	All Completely Off
$V_{TH3\_AD/FS}$<V_{FSMD}<5V or R_{FSMD}=75kΩ	Mode 3 (Note 14)	All On with 98% PWM duty cycle

Note 14: In Mode 3, the LED Open fault flag OPENF bit in 57h register will be set to '1', after exit failsafe Mode 3, need to set this bit to '0'.

10 REGISTER MAP

10.1 REGISTER MAP

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
00	CONFIG	-	-	PFS		CM	-	-	DC_PWM	R/W	0b 00000110
01	GC_CTRL	-		GCC [5:0]						R/W	0b 00111111
02	TEMP_ SEN	TRE	TRRE	-	-	-	TROF [2:0]			R/W	0b 00000000
03	PHASE_CTRL	-	-			-	-	-	PDE	R/W	0b 00000001
04~06	RSVD (Note 15)	-								-	-
07	DEFGCC	-	DEFDC_PWM	DEF_GCC[5:0]						R/W	0b 00000000
08	DEFLED1	-	-	DEFLED[6:1]						R/W	0b 00000000
09	DEFLED2	-	-	DEFLED[12:7]						R/W	0b 00000000
0B	DEFPWM1	PWM2[3:0]				PWM1[3:0]				R/W	0b 00000000
0C	DEFPWM2	PWM4[3:0]				PWM3[3:0]				R/W	0b 00000000
0D	DEFPWM3	PWM6[3:0]				PWM5[3:0]				R/W	0b 00000000
0E	DEFPWM4	PWM8[3:0]				PWM7[3:0]				R/W	0b 00000000
0F	DEFPWM5	PWM10[3:0]				PWM9[3:0]				R/W	0b 00000000
10	DEFPWM6	PWM12[3:0]				PWM11[3:0]				R/W	0b 00000000
14	SCA1	-	SCA1_DATA [6:0]							R/W	0b 01111111
15	SCA2	-	SCA2_DATA [6:0]							R/W	0b 01111111
16	SCA3	-	SCA3_DATA [6:0]							R/W	0b 01111111
17	SCA4	-	SCA4_DATA [6:0]							R/W	0b 01111111
18	SCA5	-	SCA5_DATA [6:0]							R/W	0b 01111111
19	SCA6	-	SCA6_DATA [6:0]							R/W	0b 01111111
1A	SCA7	-	SCA7_DATA [6:0]							R/W	0b 01111111
1B	SCA8	-	SCA8_DATA [6:0]							R/W	0b 01111111
1C	SCA9	-	SCA9_DATA [6:0]							R/W	0b 01111111
1D	SCA10	-	SCA10_DATA [6:0]							R/W	0b 01111111
1E	SCA11	-	SCA11_DATA [6:0]							R/W	0b 01111111
1F	SCA12	-	SCA12_DATA [6:0]							R/W	0b 01111111
20~25	RSVD (Note 15)	- (Note 16)								R/W	0b 01111111
26	PWM1_H	PWM1_DATA [11:4]								R/W	0b 00000000
27	PWM2_H	PWM2_DATA [11:4]								R/W	0b 00000000
28	PWM1_2_L	PWM2_DATA [3:0]				PWM1_DATA [3:0]				R/W	0b 00000000
29	PWM3_H	PWM3_DATA [11:4]								R/W	0b 00000000
2A	PWM4_H	PWM4_DATA [11:4]								R/W	0b 00000000
2B	PWM3_4_L	PWM4_DATA [3:0]				PWM3_DATA [3:0]				R/W	0b 00000000
2C	PWM5_H	PWM5_DATA [11:4]								R/W	0b 00000000
2D	PWM6_H	PWM6_DATA [11:4]								R/W	0b 00000000
2E	PWM5_6_L	PWM6_DATA [3:0]				PWM5_DATA [3:0]				R/W	0b 00000000
2F	PWM7_H	PWM7_DATA [11:4]								R/W	0b 00000000
30	PWM8_H	PWM8DATA [11:4]								R/W	0b 00000000
31	PWM7_8_L	PWM8_DATA [3:0]				PWM7_DATA [3:0]				R/W	0b 00000000
32	PWM9_H	PWM9_DATA [11:4]								R/W	0b 00000000
33	PWM10_H	PWM10_DATA [11:4]								R/W	0b 00000000
34	PWM9_10_L	PWM10_DATA [3:0]				PWM9_DATA [3:0]				R/W	0b 00000000
35	PWM11_H	PWM11_DATA [11:4]								R/W	0b 00000000
36	PWM12_H	PWM12_DATA [11:4]								R/W	0b 00000000
37	PWM11_12_L	PWM12_DATA [3:0]				PWM11_DATA [3:0]				R/W	0b 00000000

REGISTER MAP (CONTINUE)

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
41	LED1_2_SLS	LED2_SLSTH[3:0]				LED1_SLSTH [3:0]				R/W	0b 00000000
42	LED3_4_SLS	LED4_SLSTH[3:0]				LED3_SLSTH [3:0]				R/W	0b 00000000
43	LED5_6_SLS	LED6_SLSTH[3:0]				LED5_SLSTH [3:0]				R/W	0b 00000000
44	LED7_8_SLS	LED8_SLSTH[3:0]				LED7_SLSTH [3:0]				R/W	0b 00000000
45	LED9_10_SLS	LED10_SLSTH[3:0]				LED9_SLSTH [3:0]				R/W	0b 00000000
46	LED11_12_SLS	LED12_SLSTH[3:0]				LED11_SLSTH [3:0]				R/W	0b 00000000
4A	SYSCFG	SSCEN	SSC [1:0]		ACKEN	CMWTAP [2:0]			PWR	R/W	0b 00001000
4B	FS_FLTL	-	SHORT_FLT[2:0]			FLT_UV[3:0]				R/W	0b 00000010
4C	FLT_DET_EN	-	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	R/W	0b 00001111
4D	FLT_CONFIG	-	SHCR	OPENCR	SLSHCR	FT[3:0]				R/W	0b 01100011
4E	SHORT_FLT1	-	-	SHORT_FLT[6:1]						R	0b 00000000
4F	SHORT_FLT2	-	-	SHORT_FLT[12:7]						R	0b 00000000
51	OPEN_FLT1	-	-	OPEN_FLT[6:1]						R	0b 00000000
52	OPEN_FLT2	-	-	OPEN_FLT[12:7]						R	0b 00000000
54	SLS_FLT1	-	-	SLS_FLT[6:1]						R	0b 00000000
55	SLS_FLT2	-	-	SLS_FLT[12:7]						R	0b 00000000
57	FAULT_TYPE	TF	CRCF	RSET_SH	CMWF	TSD	SLSHORTF	SHORTF	OPENF	R/W	0b 00000000
58	RSVD	-								-	-
59	CERRCNT	CERRCNT [7:0]								R/W	0b 00000000

Note 15: "RSVD" means "Reserved". 04h~06h, 58h are not listed in the table, which is not recommended to operate.

10.2 REGISTERS DEFINITION

10.2.1 00h CONFIG Register

ADDR	REG NAME	D7:D6	D5:D4	D3	D2:D1	D0	DEFAULT
00h	CONFIG	-	PFS	CM	-	DC_PWM (Note 16)	0b 00000110

PFS PWM Frequency Setting
00 12bit, 244Hz
01 7+5bit, 24kHz
10/11 8bit, 24kHz

CM Current multiplier
0 Output current range of 33.3~100mA
1 Output current range is 1/3 of when CM='0'

DC_PWM DC or PWM output select for all outputs
0 PWM dimming. PWM duty cycle is determined by PWM registers 26h~36h
1 DC output. PWM dimming is disabled, and all outputs are DC current (I_{OUTx})

Note 16: Before enable DC_PWM mode, registers 20h~25h should set to '0x00' otherwise the OPENF bit will be set to '1'.

10.2.2 01h GC_CTRL Register

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
01h	GC_CTRL	-	GCC [5:0]	0b 00111111

GCC and SCAx control the I_{OUT} as shown in following formula:

$$I_{OUT\_F} = I_{OUT(MAX)} \times \frac{GCC}{64} \times \frac{SCAx}{128} \quad (5)$$

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \quad (6)$$
$$SCAx = \sum_{n=0}^{6} D[n] \cdot 2^n \quad (7)$$

10.2.3 02h TEMP_ SEN Register

ADDR	REG NAME	D7	D6	D5:D3	D2:D0	DEFAULT
02h	TEMP_ SEN	TRE	TRRE	-	TROF [2:0]	0b 00000000

After adding analog dimming, the current of thermal roll off will not be a fixed proportion, and the slope of roll off can be calculated by formula. $I_{ROLL} = I_{SET} \times (V_{ADJ}-V_x)/2$, (When $V_{ADJ}>2V$, $I_{ROLL} = I_{SET} \times (2V-V_x)/2$), I_{ROLL} is the current after roll off, I_{SET} is the current before roll off, V_{ADJ} is the voltage of the analog dimming pin, and Vx is the optional voltage (TROF bits) of the register.

TROF	Percentage of output current before thermal shutdown happens
000	0V
001	0.2V
010	0.4V
011	0.6V
100	0.8V
101	1.0V
110	1.2V
111	1.4V

TRRE	Thermal Roll off Report Enable at FAULTB pin
0	Do not report
1	Report

TRE	Thermal Shutdown Report Enable at FAULTB pin
0	Do not report
1	Report

10.2.4 03h PHASE_CTRL Register

ADDR	REG NAME	D7:D1	D0	DEFAULT
03h	PHASE_CTRL	-	PDE	0b 00000001

PDE	Phase delay enable
0	Disable
1	Enable (4 groups phase delay)

10.2.5 07h~10h Failsafe Program Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
07h	DEFGCC	-	DEFDC_PWM	DEF_GCC[5:0]						0b 00000000
08h	DEFLED1	-	-	DEFLED[6:1]						0b 00000000
09h	DEFLED2	-	-	DEFLED[12:7]						0b 00000000
0Bh	DEFPWM1	PWM2[3:0]				PWM1[3:0]				0b 00000000
0Ch	DEFPWM2	PWM4[3:0]				PWM3[3:0]				0b 00000000
0Dh	DEFPWM3	PWM6[3:0]				PWM5[3:0]				0b 00000000
0Eh	DEFPWM4	PWM8[3:0]				PWM7[3:0]				0b 00000000
0Fh	DEFPWM5	PWM10[3:0]				PWM9[3:0]				0b 00000000
10h	DEFPWM6	PWM12[3:0]				PWM11[3:0]				0b 00000000

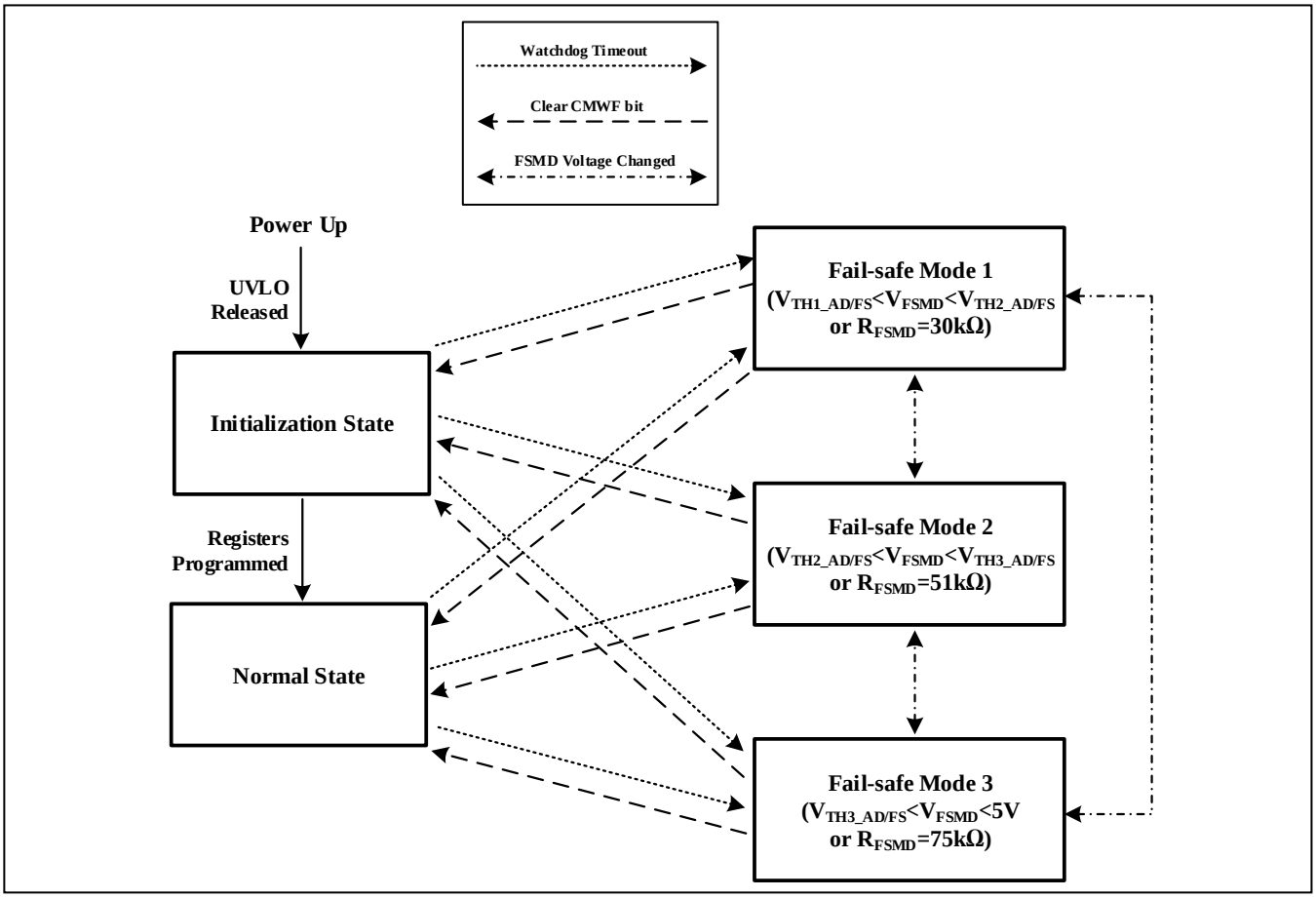


Figure 25 Operation States

10.2.6 14h~1Fh Scaling Registers

ADDR	REG NAME	D7	D6:D0	DEFAULT
14h	SCA1	-	SCA1_DATA [6:0]	0b 01111111
15h	SCA2	-	SCA2_DATA [6:0]	0b 01111111
16h	SCA3	-	SCA3_DATA [6:0]	0b 01111111
17h	SCA4	-	SCA4_DATA [6:0]	0b 01111111
18h	SCA5	-	SCA5_DATA [6:0]	0b 01111111
19h	SCA6	-	SCA6_DATA [6:0]	0b 01111111
1Ah	SCA7	-	SCA7_DATA [6:0]	0b 01111111
1Bh	SCA8	-	SCA8_DATA [6:0]	0b 01111111
1Ch	SCA9	-	SCA9_DATA [6:0]	0b 01111111
1Dh	SCA10	-	SCA10_DATA [6:0]	0b 01111111
1Eh	SCA11	-	SCA11_DATA [6:0]	0b 01111111
1Fh	SCA12	-	SCA12_DATA [6:0]	0b 01111111

The 7-bit Scaling Registers SCAx (14h~1Fh) individually set the DC output current of each channel.

GCC[5:0] and SCAx control the OUTx current (I_{OUTx}) as shown in following equation:

$$I_{OUTx} = I_{OUT\_FU} \times \frac{GCC}{64} \times \frac{SCAx}{128} \qquad (5)$$

Where, x is from 1 to 12 for different output channel.

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \qquad (6)$$

$$SCAx = \sum_{n=0}^{6} D[n] \cdot 2^n \qquad (7)$$

10.2.7 26h~37h PWM Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
26h	PWM1_H	PWM1_DATA [11:4]								0b 00000000
27h	PWM2_H	PWM2_DATA [11:4]								0b 00000000
28h	PWM1_2_L	PWM2_DATA [3:0]				PWM1_DATA [3:0]				0b 00000000
29h	PWM3_H	PWM3_DATA [11:4]								0b 00000000
2Ah	PWM4_H	PWM4_DATA [11:4]								0b 00000000
2Bh	PWM3_4_L	PWM4_DATA [3:0]				PWM3_DATA [3:0]				0b 00000000
2Ch	PWM5_H	PWM5_DATA [11:4]								0b 00000000
2Dh	PWM6_H	PWM6_DATA [11:4]								0b 00000000
2Eh	PWM5_6_L	PWM6_DATA [3:0]				PWM5_DATA [3:0]				0b 00000000
2Fh	PWM7_H	PWM7_DATA [11:4]								0b 00000000
30h	PWM8_H	PWM8DATA [11:4]								0b 00000000
31h	PWM7_8_L	PWM8_DATA [3:0]				PWM7_DATA [3:0]				0b 00000000
32h	PWM9_H	PWM9_DATA [11:4]								0b 00000000
33h	PWM10_H	PWM10_DATA [11:4]								0b 00000000
34h	PWM9_10_L	PWM10_DATA [3:0]				PWM9_DATA [3:0]				0b 00000000
35h	PWM11_H	PWM11_DATA [11:4]								0b 00000000
36h	PWM12_H	PWM12_DATA [11:4]								0b 00000000
37h	PWM11_12_L	PWM12_DATA [3:0]				PWM11_DATA [3:0]				0b 00000000

Note 17: To ensure the accuracy of results in single-LED short detect, LED-short detect and LED-open detect, the PWM value should be more than 25%. For example, if PWM mode is 8-bit, the PWM value should be more than 0x40.

Each OUTx has 12-bit (or 7+5-bit) to modulate the PWM duty cycle in 4096 steps. The value of the PWM Registers decides the average current of each OUTx LED noted I_{LED}.

I_{LED} computed by following formula:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (8)$$

Where, D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (26h~40h), in 12bit or 7+5-bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{11} D[n] \cdot 2^n}{4096} \qquad (9)$$

In 8bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=4}^{11} D[n] \cdot 2^n}{256} \qquad (10)$$

10.2.8 41h~46h Single LED Short Threshold Setting Registers

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
41h	LED1_2_SLS	LED2_SLSTH[3:0]	LED1_SLSTH [3:0]	0b 00000000
42h	LED3_4_SLS	LED4_SLSTH[3:0]	LED3_SLSTH [3:0]	0b 00000000
43h	LED5_6_SLS	LED6_SLSTH[3:0]	LED5_SLSTH [3:0]	0b 00000000
44h	LED7_8_SLS	LED8_SLSTH[3:0]	LED7_SLSTH [3:0]	0b 00000000
45h	LED9_10_SLS	LED10_SLSTH[3:0]	LED9_SLSTH [3:0]	0b 00000000
46h	LED11_12_SLS	LED12_SLSTH[3:0]	LED11_SLSTH [3:0]	0b 00000000

LEDx_SLSTH sets the single LED short detection threshold for each channel, V_{SLSTH}, and to detect the result correctly, V_{SLSTH} should be set to be smaller than channel voltage when single LED short or make LED+ supply voltage higher.

For example:

Condition 1, If LED+ supply voltage is 14V, LED V_f is 2.6V, and channel voltage is 11.4V(=14V-2.6V), so the V_{SLSTH} suggest to set as 10.2V(LEDx_SLSTH = "1011").

Condition 2, if channel is only with one LED and LED V_f is 1.8~2.5V, suggest that the LED+ supply voltage is higher than 2.5V to make sure the detect result is correct.

LEDx_SLSTH	Singe LED short threshold voltage
0000	2.5V
0001	3.2V
0010	3.9V
0011	4.6V
0100	5.3V
0101	6.0V
0110	6.7V
0111	7.4V
1000	8.1V
1001	8.8V
1010	9.5V
1011	10.2V
1100	11.4V
1101	12.6V
1110	13.8V
1111	15.0V

10.2.9 4Ah System Configuration Register (SYSCFG) – Read/Write

ADDR	REG NAME	D7	D6:D5	D4	D3:D1	D0	DEFAULT
4Ah	SYSCFG	SSCEN	SSC [1:0]	ACKEN	CMWTAP [2:0]	PWR	0b 00001000

ACKEN	Acknowledge Enable
0	No acknowledge is transmitted following successfully received writes
1	Acknowledge (0x7F) is transmitted following successfully received writes

PWR	This bit is reset to 0 upon power-up. It may be written to a 1 by the MCU. Reading this bit allows the MCU to detect if there has been a power cycle.
0	A power cycle has occurred since last write to a '1'
1	No power cycle has occurred since the last write to a '1'

CMWTAP [2:0] This 3-bit value selects the tap point (i.e., bit number, starting from 0) on the 24-bit communications watchdog timer to establish the time-out condition.

CMWTAP [2:0]	Time-Out Time
7	1024ms
6	512ms
5	256ms
4	128ms (Default)
3	64ms
2	32ms
1	16ms
0	8ms

SSCEN	Spread Spectrum Enable
0	Disable
1	Enable-not allowed when PWM frequency is 244Hz

SSC	Spread Spectrum frequency Range
00	125Hz
01	250Hz
10	500Hz
11	1kHz

10.2.10 4Bh FS_FLTL Register

ADDR	REG NAME	D7	D6:D4	D3:D0	DEFAULT
4Bh	FS_FLTL	-	SHORT_FLT	FLT_UV	0b 00000100

FLT_UV set UVLO threshold V_{FLT_UV} for the LED open fault detection and single LED short fault detec false fault triggering due to insufficient power supply voltage.tion to prevent

SHORT_FLT sets the LED string short detection threshold, V_{SC}, and to detect the result correctly, V_{SC} should be set to be smaller than LED+ supply voltage.

For example:

Condition 1, if LED+ supply voltage is 14V, the V_{SC} suggest setting to be V_{IN}-1V(SHORT_FLT = “000”) or 12V (SHORT_FLT = “101”).

Condition 2, if LED+ supply voltage is 10V, the V_{SC} suggest setting to be V_{IN}-1V(SHORT_FLT = “000”) or 8V (SHORT_FLT = “110”).

FLT_UV	UVLO threshold voltage for the LED open fault detection and single LED short fault detection
0000	4.5V
0001	5V
0010	6V
0011	7V
0100	8V
0101	9V
0110	10V
0111	11V
1000	12V
1001	13V
1010	14V
1011	15V
1100	16V
1101	16V
1110	16V
1111	16V

SHORT_FLT	LED short threshold voltage
000	VIN-1V
001	10V
010	6V
011	14V
100	5V
101	12V
110	8V
111	Reserve

10.2.11 4Ch Diagnostic Register

ADDR	REG NAME	D7:D6	D5	D4	D3	D2	D1	D0	DEFAULT
4Ch	FLT_DET_EN	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	0b 00001111

SLSDF Single LED Short Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

SLSDE Single LED Short Detect Enable
0 Detect disabled
1 Detect enabled

SDF Short Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

SDE Short Detect Enable
0 Detect disabled
1 Detect enabled

ODF Open Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

ODE Open Detect Enable
0 Detect disabled
1 Detect enabled

10.2.12 4Dh~55h Diagnostic Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
4Dh	FLT_CONFIG	-	SHCR	OPENCR	SLSHCR	FT[3:0]				0b 01100011
4Eh	SHORT_FLT1	-	-	SHORT_FLT[6:1]						0b 00000000
4Fh	SHORT_FLT2	-	-	SHORT_FLT[12:7]						0b 00000000
51h	OPEN_FLT1	-	-	OPEN_FLT[6:1]						0b 00000000
52h	OPEN_FLT2	-	-	OPEN_FLT[12:7]						0b 00000000
54h	SLS_FLT1	-	-	SLS_FLT[6:1]						0b 00000000
55h	SLS_FLT2	-	-	SLS_FLT[12:7]						0b 00000000

FT Fault report delay time setting
0000 32us
0001 64us
0010 128us
0011 256us
0100 512us
0101 1.024ms
0110 2.048ms
0111 4.096ms
1000 7.8125ms
1001 15.625ms
1010 31.25ms
1011 62.5ms

1100 0.125s
1101 0.25s
1110 0.5s
1111 1s

SLSHCR single LED short output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

SHCR LED short output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

OPENCR LED OPEN output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

SHORT_FLTx LED string short fault flag for each OUT1~OUT12
0 No LED string shorted
1 LED string shorted

OPEN_FLTx LED string open fault flag for each OUT1~OUT12
0 No LED string open
1 LED string open

SLS_FLTx Single LED short fault flag for each OUT1~OUT12
0 No single LED shorted
1 Single LED shorted

10.2.13 57h Fault Type Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
57h	FAULT_TYPE	TF	CRCF	RSET_SH	CMWF	TSD	SLSHORTF	SHORTF	OPENF	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

TF Thermal rolloff fault flag
0 No thermal rolloff
1 Thermal rolloff

RSET_SH ISET pin short fault flag
0 No short
1 Shorted

CRCF Interface communication Check Sum Failure fault flag
0 No communication Check Sum Failure
1 Communication Check Sum Failure

CMWF Communication Time-Out fault flag
0 No communication time-out
1 Communication time-out

TSD Thermal shutdown fault flag
0 No thermal shutdown
1 Thermal shutdown

SLSHORTF Single LED Short fault flag. Any out occurs single LED short, this bit will set to 1.
0 No single LED short
1 Single LED short

SHORTF LED Short fault flag. Any out occurs LED short, this bit will set to 1.
0 No LED short
1 LED short

OPENF LED Open fault flag. Any out occurs LED open, this bit will set to 1.
0 No LED open
1 LED open

Note 18: In failsafe Mode 3, the OPENF bit will be set to '1', after exit failsafe Mode 3, need to set this bit to '0'.

10.2.14 Diagnostic Register (Continue)

ADDR	REG NAME	D7:D0	DEFAULT
59h	CERRCNT	CERRCNT [7:0]	0b 00000000

This register value is incremented each time a CRC error is received. This register may be read by the MCU and then written back to 0 to clear the count. The CERRCNT value saturates at FFh; it does not wrap back to 0 when it reaches FFh. The CERRCNT register is not automatically cleared when a communications reset is received. It must be cleared manually by writing it back to 0. Note that the CERRCNT register can be written to any 8-bit value. This is intended for diagnostic purposes.

11 CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

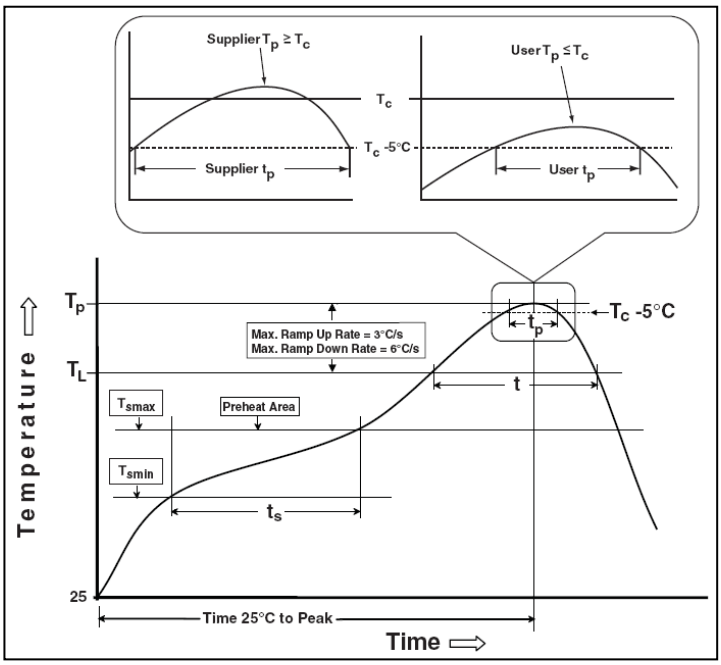
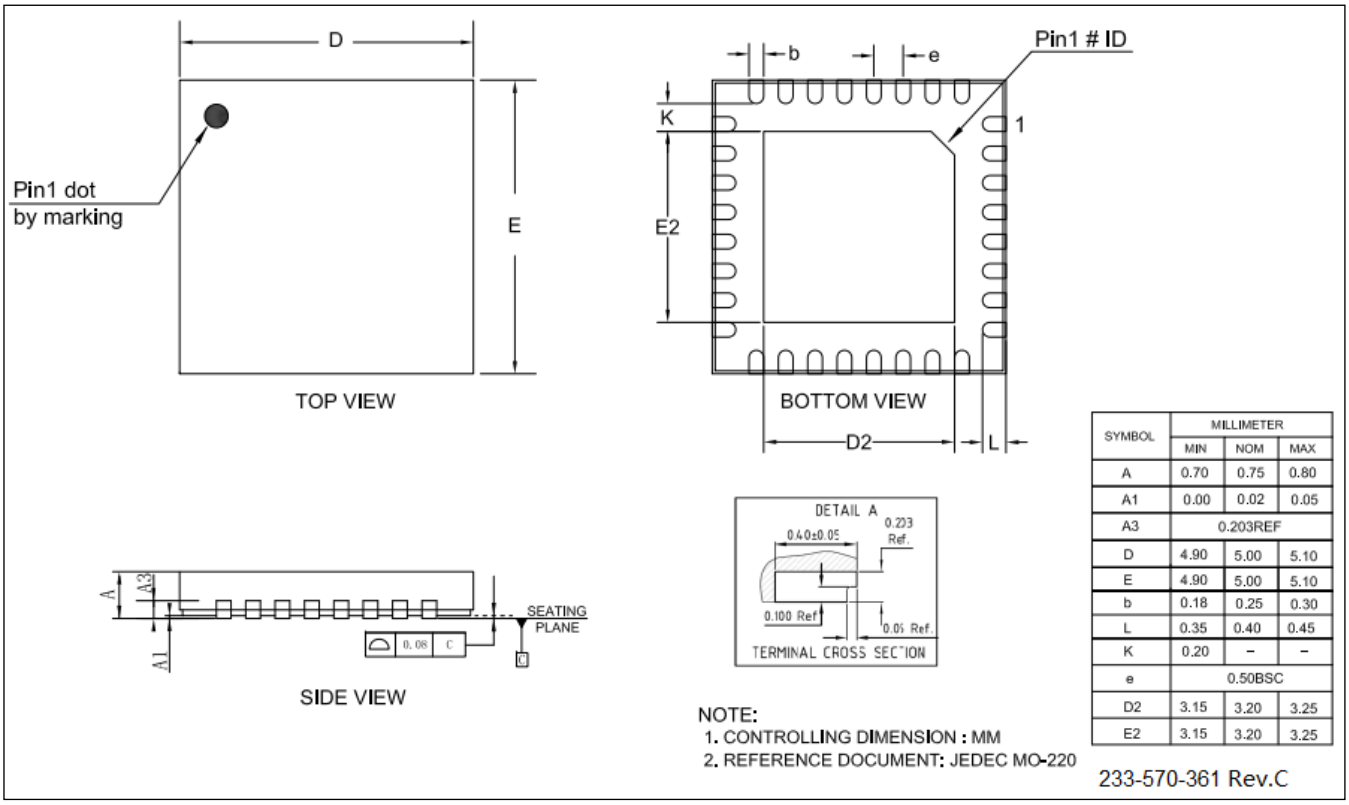


Figure 26 Classification Profile

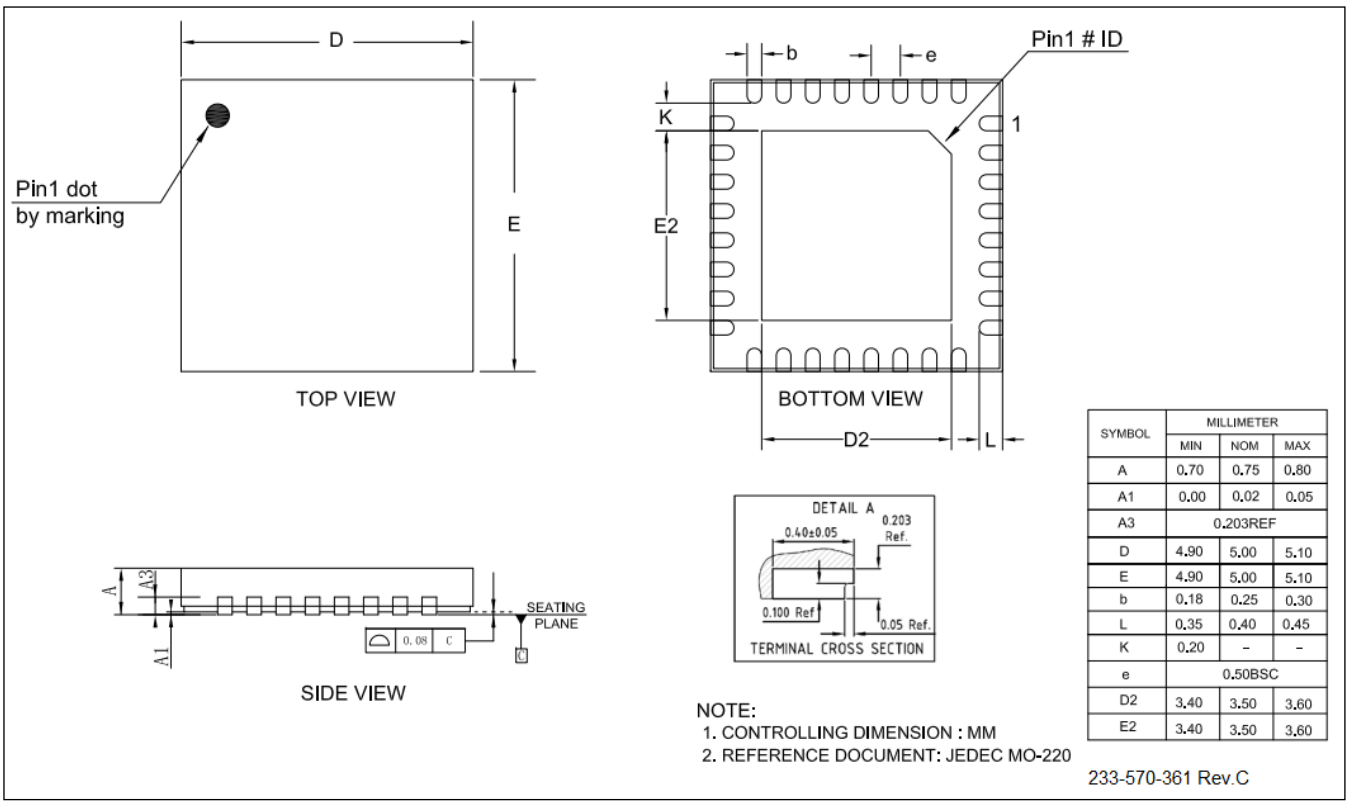
12 PACKAGE INFORMATION

WFQFN-32 (IS32LT3137-QWLA3-TR)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20	–	–
e		0.50BSC	
D2	3.15	3.20	3.25
E2	3.15	3.20	3.25

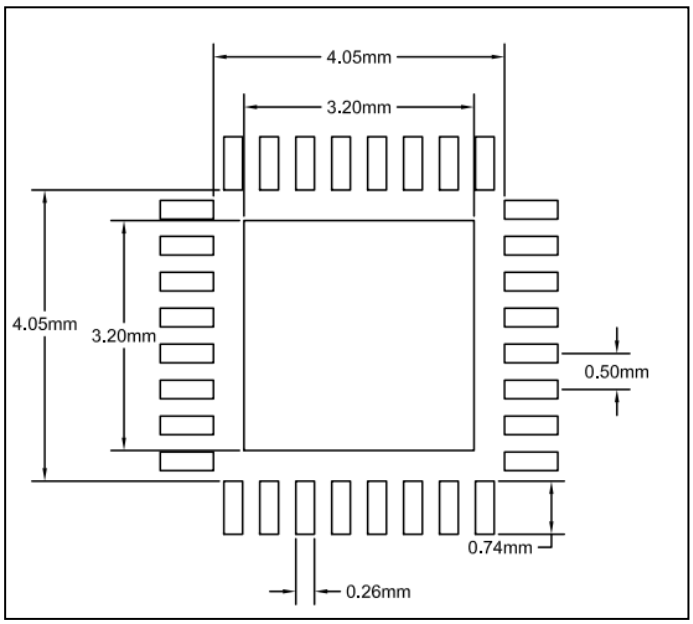
WFQFN-32 (IS32LT3137-QWLCA3-TR) (With Copper Wire Bonding)



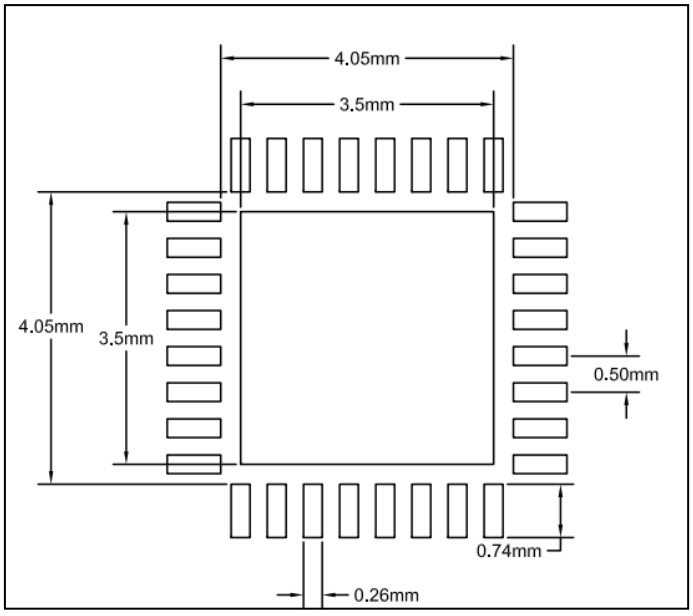
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20	-	-
e		0.50BSC	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60

13 RECOMMENDED LAND PATTERN

WFQFN-32 (IS32LT3137-QWLA3-TR)



WFQFN-32 (IS32LT3137-QWLCA3-TR) (With Copper Wire Bonding)



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

14 REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2023.07.04
B	1.Add Note 2 about IS32LT3137-QWLCA3-TR is with copper wire bonding 2.Add Note 9 about reconnect TX or RX's CRC error issue 3.Add Note 13 about Device ID detect 4.Add Note 17 about ensuring LED open/short detect and single LED short detection accuracy 5.Add Package Information for IS32LT3137-QWLCA3-TR(with copper wire bonding) 6.Add Recommended Land Pattern for IS32LT3137-QWLCA3-TR(with copper wire bonding)	2024.05.14