IS32FL3749

LOCAL DIMMING 24×4 MATRIX LED DRIVER

July 2024

GENERAL DESCRIPTIONS

IS32FL3749 is a matrix LED driver with 24 high voltage (16V) constant current channels. It supports from one to four power scan to become a 24×n (n=1~4) matrix LED driver. Each LED can be pulse width modulated (PWM) with maximum 16-bit precision for smooth LED brightness control. In addition, each LED can be controlled by an 8-bit output current control register (Dot correction, current scale, SL), which allows fine tuning the current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel is designed to be 60mA, which can be adjusted by three 8-bit global control registers group (one group for R for CS 3×n, one group for G for channels 3×n+1, and one group for B for channels 3×n+2, n=0~7, for example: one group for R is CS0,CS3,……CS18,CS21 one group for G is CS1,CS4,……CS19,CS22 one group for B is CS2,CS5,……CS20,CS23). Proprietary algorithms are used in IS32FL3749 to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor. All registers can be programmed via VSB (video series bus, up to 33MHz) or SPI (up to 33MHz) bus.

IS32FL3749 can be turned off with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature. It internally generates 4.8V V_{LDOOUT} to power the internal logic operation, which can also be external powered from 3V to 5.5V.

IS32FL3749 is available in eTQFP-48 (7mm × 7mm) package and can work over temperature range from -40°C to +125°C.

FEATURES

- Support 24 constant current channels, 60mA/ch
- Tolerate up to 18V, nominal operation voltage between 4.3V to 16V, multiple LED's can be connected in series
- Built-in LDO to generate 4.8V supply for internal logic
- Interface
  - VSB (video serial bus, 33MHz)
  - SPI (33MHz)
- Reset register reset all the registers to default
- Support 8-bit, 16-bit, 8+4-bit dithering and 8+8-bit dithering PWM mode
- Built-in Dot correction: 8-bit/dot
- 8-bit × 3 global current adjustment
- 4 groups delay to minimize the power ripple
- Support bi-directional data output via DI
- PSW short protection
- Spread spectrum
- Programmable detection of open/short, detected LED and store detected LED information in registers for ease of manufacturing/debugging
- Low standby and sleep mode current
- For matrix scanning operation
  - Built-in de-ghosting circuit
  - Reduced inactive LED reverse bias to improve LED reliability
- Over temperature protection
- Operating temperature: -40°C to 125°C
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- eTQFP-48 (7mm × 7mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Mini LED Back Light
- Automotive LED Back Light
- Automotive Center Information Display
- Automotive Cluster Display

TYPICAL APPLICATION CIRCUIT

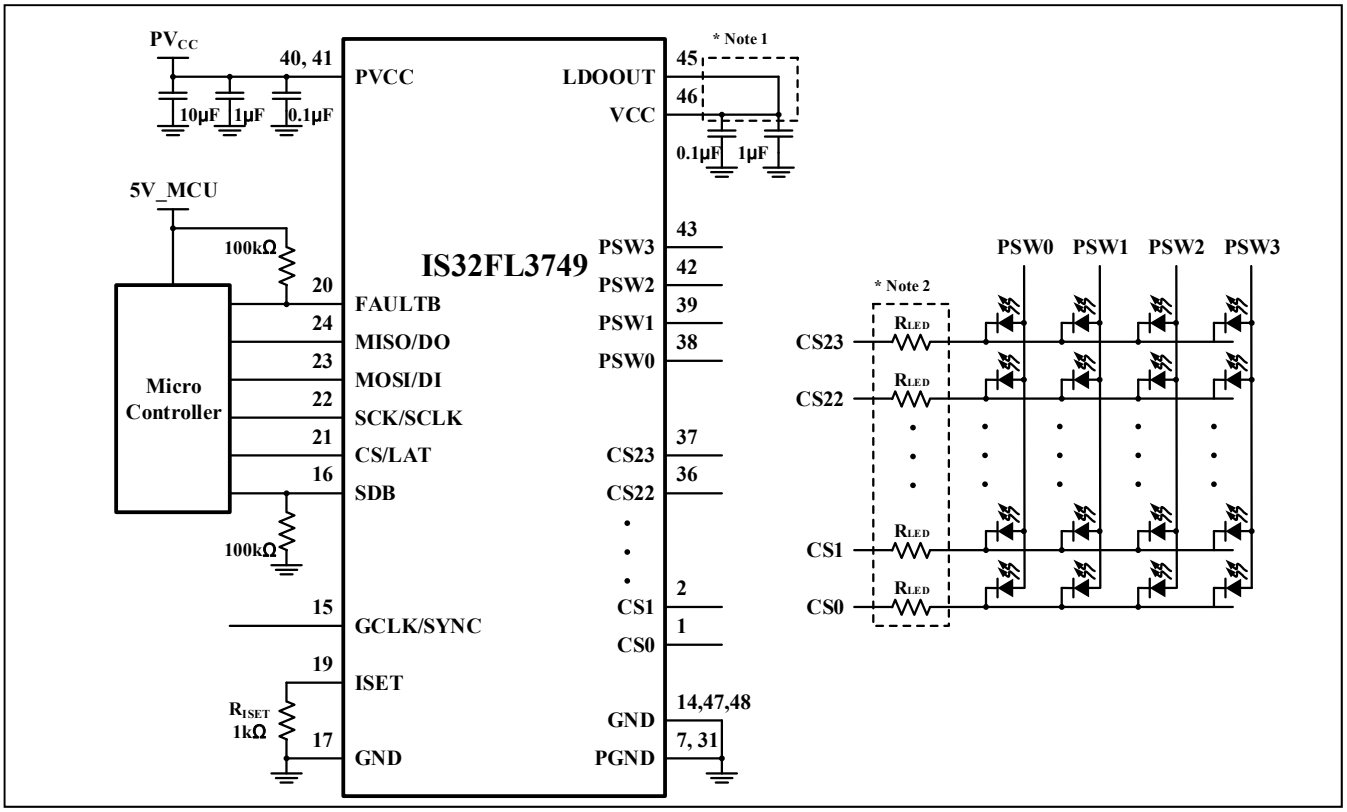


Figure 1 Typical Application Circuit: VSB/SPI Interface, 24×4 Array

TYPICAL APPLICATION CIRCUIT (CONTINUED)

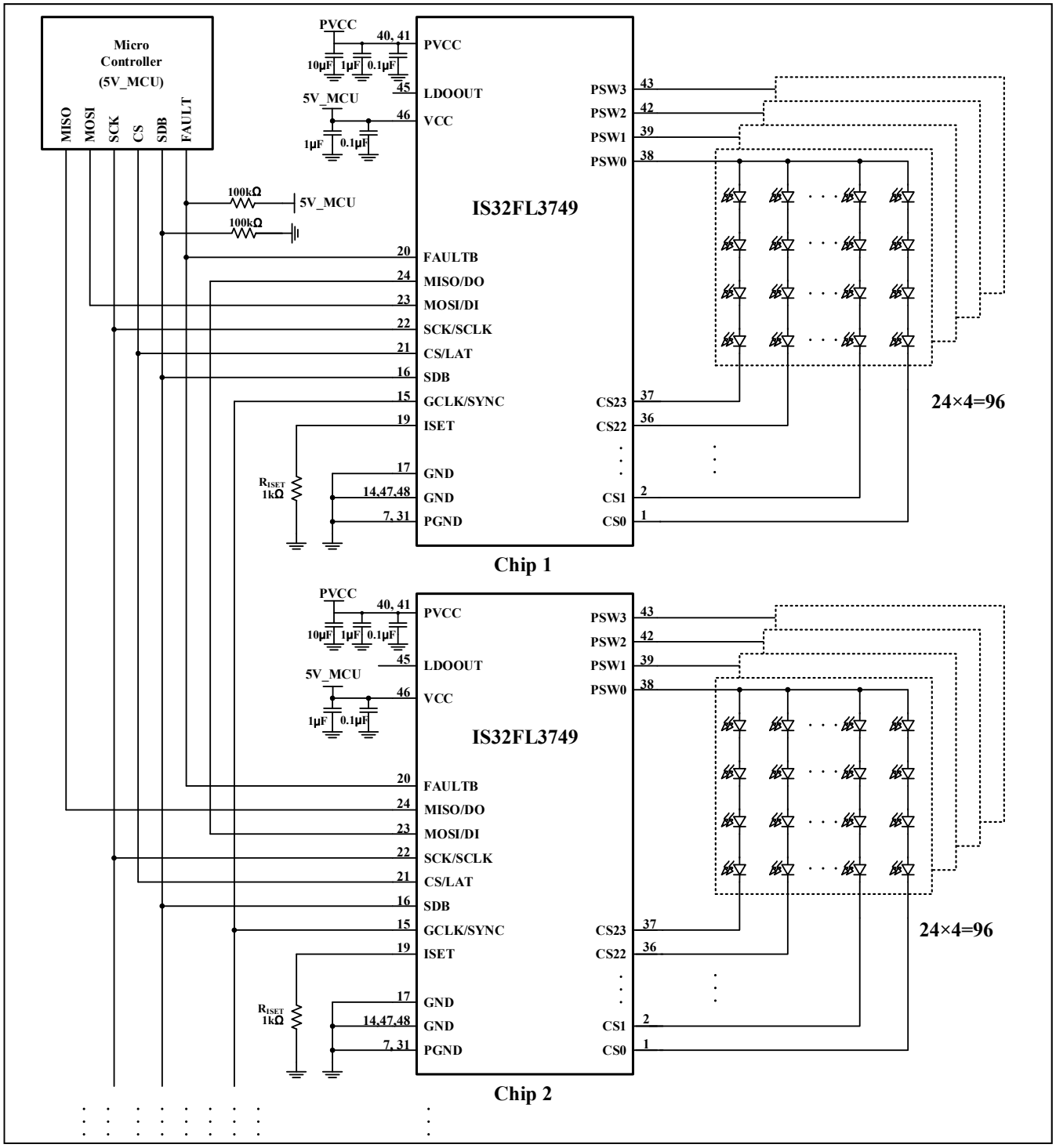
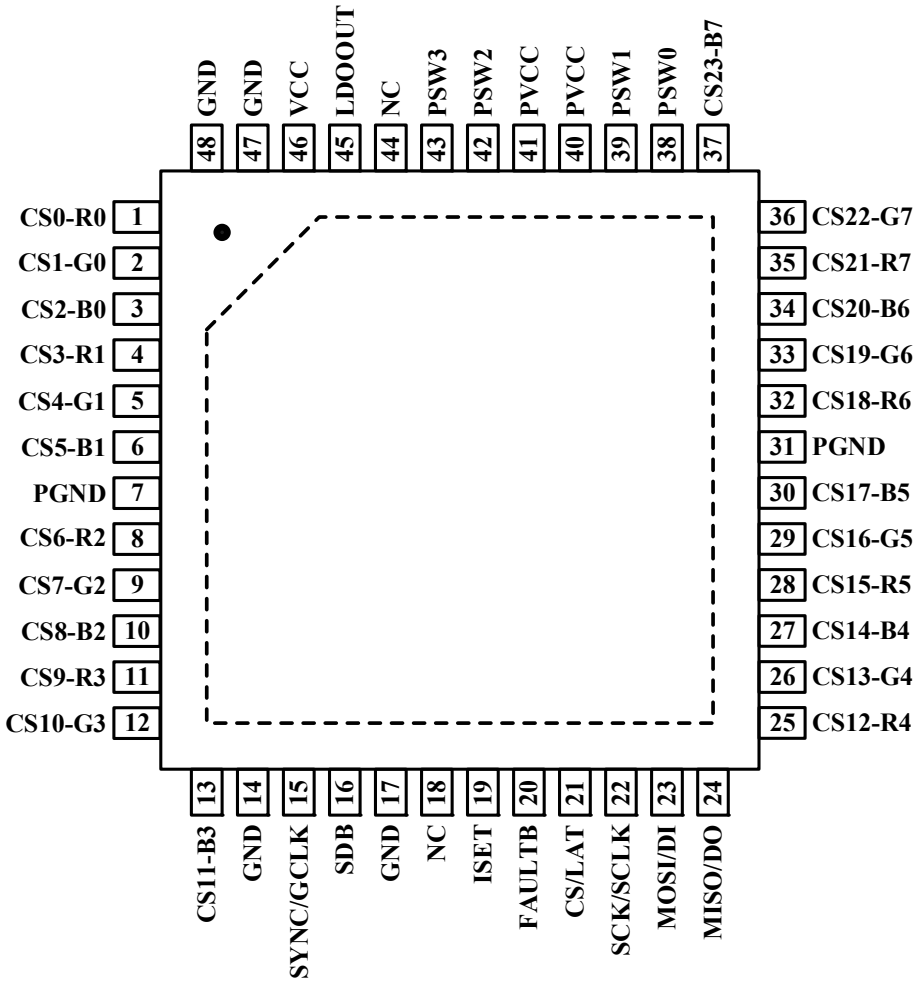


Figure 2 Typical Application Circuit (Cascade)

Note 1: LDOOUT can provide stable 4.8V power supply, which can directly supply power to VCC (LDO is short to VCC), and LDOOUT will turn off the output when enter hardware shutdown mode (V_{SDB}=0V). When LDOOUT is not used, LDOOUT pin can be float/NC.

Note 2: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS32FL3749, it is determined by PV_{CC}, I_{OUT}, V_F of LED, V_{HR} of PSW_x and CS_y. $R_{LED}=(PV_{CC}-V_F-V_{HRPSW}-VHR_{CS})/I_{OUT}$.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTQFP-48	

PIN DESCRIPTION

No.	Pin	Description
1~6,8~13, 25~30,32~37	CS[23:0]	Current sink pin for LED matrix.
7,31	PGND	Power GND.
14,17,47,48	GND	Analog GND.
15	SYNC/GCLK	Synchronization.
16	SDB	Shutdown pin.
18, 44	NC	Not connect.
19	ISET	Set the maximum I_{OUT} current.
20	FAULTB	Fault report pin. Register DEh can read the function of the FAULTB pin and active low when the fault event happens. Can be NC (float) if fault function is not used.
21	CS / LAT	CS signal of SPI / Latch signal of VSB.
22	SCK / SCLK	SPI clock / VSB clock.
23	MOSI / DI	SPI input data / VSB input data.
24	MISO / DO	SPI output data / VSB output data.
38,39,42,43	PSW[3:0]	Power PSW.
40,41	PVCC	Power for current source PSWx.
45	LDOOUT	LDO output, 4.8V typical.
46	VCC	Analog and digital circuits.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32FL3749-TQLA3-TR IS32FL3749-TQLCA3-TR (Note 3)	eTQFP-48, Lead-free	2500

Note 3: IS32FL3749-TQLCA3-TR is with copper wire bonding.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Supply voltage, PV_{CC}	-0.3V ~ +20V
Voltage at CSy pin	-0.3V ~ +20V
Voltage at any input pin	-0.3V ~ PV_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	38.9°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	7.567°C/W
ESD (HBM) ESD (CDM)	±3kV ±750V

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.

"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.

The following specifications apply for PV_{CC}= 12V, V_{CC}= 5V, T_A= 25°C, unless otherwise noted (Note 5).

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
PV_{CC}	Power supply voltage			4.3		16	V
V_{CC}	Supply voltage			3.0		5.5	V
$I_{CC}(PV_{CC})$	Quiescent power supply current	R_{ISET}=1.0kΩ, PV_{CC}=12V, V_{SDB}=V_{CC}=5V, OSC=16MHz, all LEDs off			2	5.5	mA
$I_{CC}(V_{CC})$		R_{ISET}=1.0kΩ, PV_{CC}=12V, V_{SDB}=V_{CC}=5V, OSC=16MHz, all LEDs off			8.0	10	mA
$I_{SD}(PV_{CC})$	Shutdown current	PV_{CC}=12V, V_{CC}=5V, V_{SDB}=0V, OSC=16MHz			10	15	µA
$I_{SD}(V_{CC})$					3	7	
$I_{SD}(PV_{CC})$		PV_{CC}=12V, V_{SDB}=V_{CC}=5V, OSC=16MHz, SSD=1			450	600	µA
$I_{SD}(V_{CC})$					160	300	
I_{OUT}	Maximum constant current of CSy	R_{ISET}=1kΩ, GCCR= GCCG= GCCB=0xFF, SL=0xFF, PWM=0xFFFF, V_{OUT}= 0.8V	♦	57.5	60	62.5	mA
			◊	56	60	64	mA
ΔI_{MAT}	Output current fault between outputs (Note 6)	R_{ISET}=1kΩ, GCCR= GCCG= GCCB=0xFF, SL=0xFF, PWM=0xFFFF, V_{OUT}= 0.8V	♦	-5		5	%
			◊	-7		7	%
ΔI_{ACC}	Output current fault between devices (Note 7)	R_{ISET}=1kΩ, GCCR= GCCG= GCCB=0xFF, SL=0xFF, PWM=0xFFFF, V_{OUT}= 0.8V	♦	-5		5	%
			◊	-7		7	%
I_{OZ}	Output leakage current	PWM= 0x0000, V_{OUT}= 16V	♦			0.2	µA
			◊			0.7	µA
I_{LDO_MAX}	LDOOUT output current capability	PV_{CC}≥ 12V, V_{LDO}> 4.5V				50	mA
V_{HR}	Current switch headroom voltage PSWx	R_{ISET}= 1kΩ, $I_{PSWITCH}$= 0.8A, GCCR= GCCG= GCCB=0xFF, SL=0xFF, PWM=0xFFFF			0.4	0.65	V
	Current sink headroom voltage CSy	R_{ISET}= 1kΩ, I_{SINK}= 60mA, GCCR= GCCG= GCCB=0xFF, SL=0xFF, PWM=0xFFFF			0.35	0.5	

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for PV_{CC}= 12V, V_{CC}= 5V, T_A= 25°C, unless otherwise noted (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SCAN}	Period of PSW_X scanning	OSC=16MHz, 16-bit PWM Mode	3.5	4.096	4.5	ms
		OSC=16MHz, 8+8-bit/8+4-bit/8-bit PWM Mode	15.8	17.3	19.3	μs
t_{CSON}	CS-ON time during scan, the CSy are all on during this time	OSC=16MHz, 16-bit PWM Mode	3.5	4.095	4.5	ms
		OSC=16MHz, 8+8-bit/8+4-bit/8-bit PWM Mode	15	16.8	18.5	μs
t_{NOL1}	Non-overlap blanking time during scan, the PSWx and CSy are all off during this time	OSC=16MHz		0.3		μs
t_{NOL2}	Delay total time for CS1 to CS 24, during this time, the PSWx is on but CSy is not all turned on	OSC=16MHz (Note 8)		0.2		μs
T_{SD}	Thermal shutdown	(Note 8)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 8)		20		°C
V_{OD}	LED open detect threshold	PV_{CC}=12V, V_{CC}=5V, R_{ISET}=1kΩ, I_{OUT}≥0.1mA, PWM> 40%, measured at CSy	0.08	0.15		V
V_{SD}	LED short detect threshold	PV_{CC}=12V, V_{CC}=5V, R_{ISET}=1kΩ, I_{OUT}≥0.1mA, PWM> 40%, measured at CSy		0.925× PV_{CC}	0.98× PV_{CC}	V
Logic Electrical Characteristics (MOSI/DI, MISO/DO, CS/LAT, SCK/SCLK, SDB)						
V_{IL}	Logic “0” input voltage (not include SDB pin)	V_{CC}= 3.0V~5.5V			0.25V_{CC}	V
V_{IH}	Logic “1” input voltage (not include SDB pin)	V_{CC}= 3.0V~5.5V	0.7V_{CC}			V
V_{HYS}	Input Schmitt trigger hysteresis (not include SDB pin)	V_{CC}= 3.6V		0.2		V
V_{OH}	H level MISO/DO pin output voltage	I_{OH}= -8mA (Note 8)	V_{CC}-0.4V		V_{CC}	V
V_{OL}	L level MISO/DO pin output voltage	I_{OL}= 8mA (Note 8)	0		0.4	V
V_{IL_SDB}	Logic “0” input voltage	V_{CC}= 3.0V~5.5V			0.6	V
V_{IH_SDB}	Logic “1” input voltage	V_{CC}= 3.0V~5.5V	2			V
I_{IL}	Logic “0” input current	V_{INPUT}= L (Note 8)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= H (Note 8)		5		nA

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 8)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		33	MHz
t_{CH}	Clock high pulse duration	10			ns
t_{CL}	Clock low pulse duration	10			ns
t_{SICH}	MOSI to Clock rising edge setup time	5			ns
t_{CLCH}	CS falling edge to Clock rising edge	33			ns
t_{CHSI}	Clock rising edge to MOSI hold time	3			ns
t_{CLCH}	Clock falling edge to CS rising edge hold time	10			ns
t_{CSH}	CS high pulse duration	60			ns
t_{SOR}	MISO rise time		3		ns
t_{SOF}	MISO fall time		3		ns
t_{CHSO}	Clock rising edge to MISO		30		ns

DIGITAL INPUT VSB PSWITCHING CHARACTERISTICS (NOTE 8)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		33	MHz
t_{CH}	Clock high pulse duration	10			ns
t_{CL}	Clock low pulse duration	10			ns
t_{DICH}	DI to Clock rising edge setup time	5			ns
t_{LLCH}	LAT falling edge to Clock rising edge	33			ns
t_{CHDI}	Clock rising edge to DI hold time	3			ns
t_{CLLH}	Clock falling edge to LAT rising edge hold time	10			ns
t_{LH}	LAT high pulse duration	60			ns
t_{DOR}	DO rise time		3		ns
t_{DOF}	DO fall time		3		ns
t_{CHDO}	Clock rising edge to DO		30		ns

Note 5: Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

Note 6: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = MAX\left(ABS\left(\frac{I_{OUTn}(n=0\sim23)}{\frac{I_{OUT0}+I_{OUT1}+\cdots+I_{OUT23}}{24}} - 1 \right) \right) \times 100\%$$

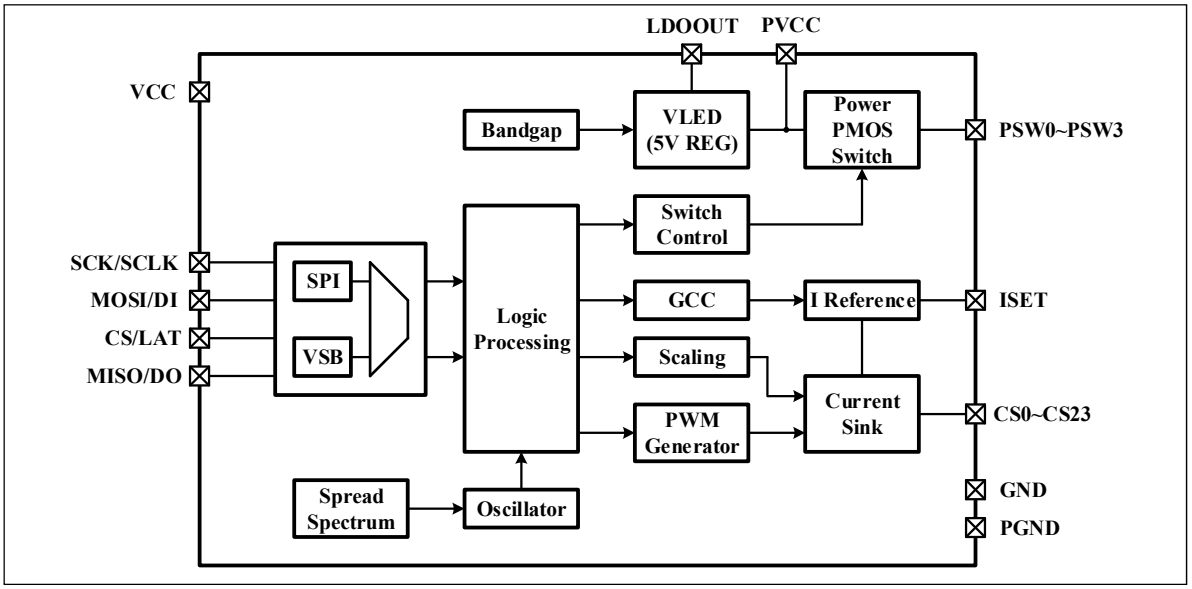
Note 7: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{OUT} = ABS\left(\frac{\frac{I_{OUT0}+I_{OUT1}+\cdots+I_{OUT23}}{24} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 60mA when R_{ISET}= 1kΩ.

Note 8: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

IS32FL3749 support SPI interface and VSB (Video serial bus) interface.

SPI INTERFACE

IS32FL3749 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS32FL3749 latches data when CS is asserted (low to high).

The maximum SCK frequency supported in IS32FL3749 is 33MHz.

WRITING OPERATION

SPI write data format is 8-bit (byte) command followed by the register data. The command byte determines the length and function of the register data.

When writing Update/Reset/Fault Flag Clear Register to IS32FL3249, only the command is sent (without data). The IS32FL3749 SPI write register timing as shown in figure 4~7.

READING OPERATION

FC0, FC1, fault status, open/short detect result registers can be read by SPI.

To read the registers, the first command byte selects the corresponding register, followed by a CS pulse to latch after read command byte is written to IS32FL3749. Read register timing as shown in figure 8/10, read the MISO data after sending the read command byte.

All register writes and read command as shown in Table 1.

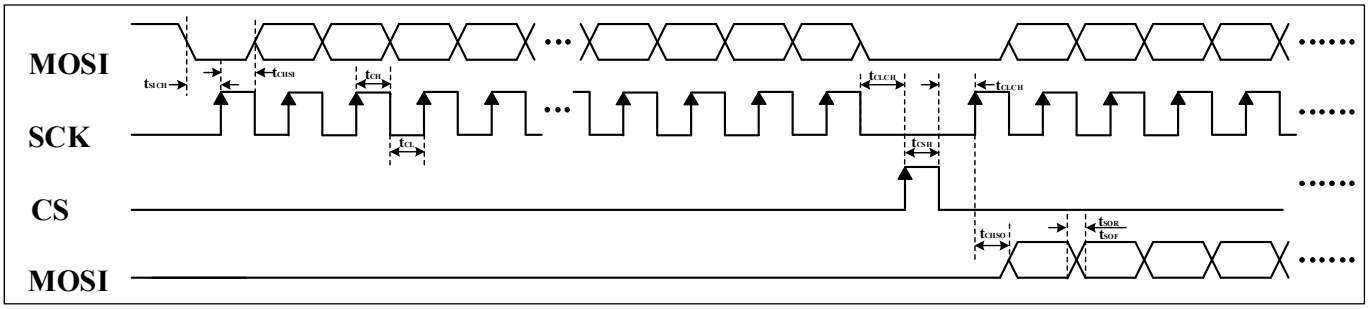


Figure 3 SPI Input Timing

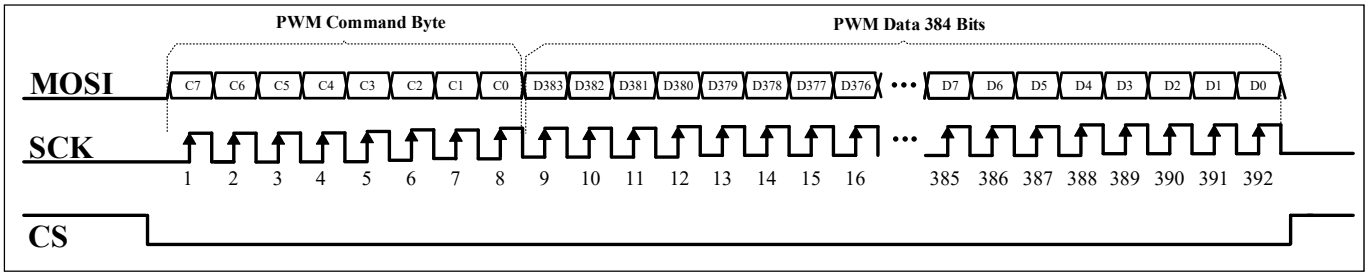


Figure 4 SPI Writing PWM Register Data to IS32FL3749

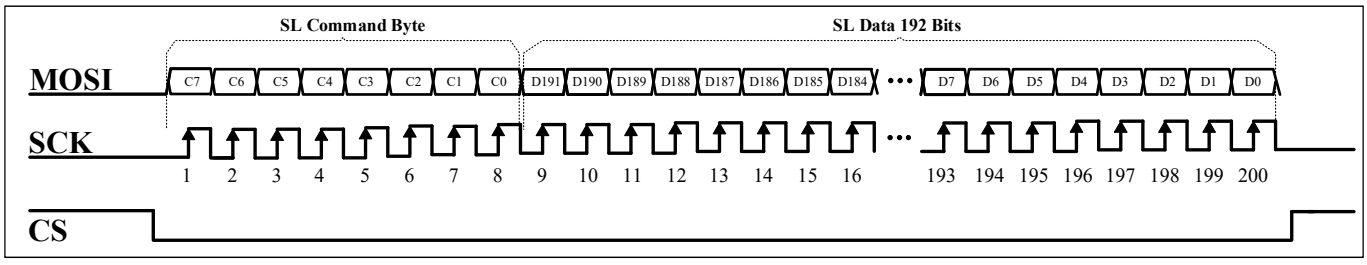


Figure 5 SPI Writing Scaling Register Data to IS32FL3749

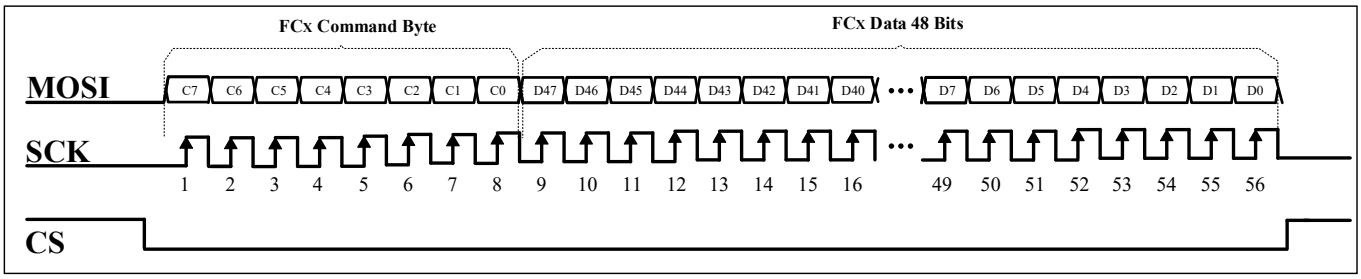


Figure 6 SPI Writing FCx Register Data to IS32FL3749

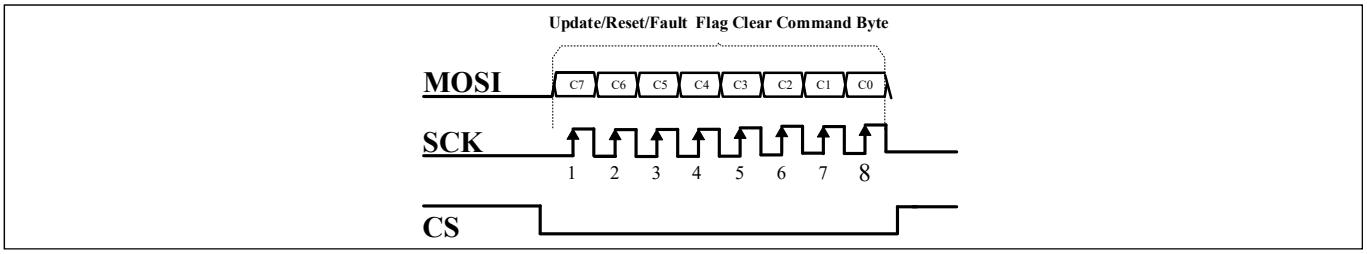


Figure 7 SPI Writing Update/Reset/Fault Flag Clear Register Data to IS32FL3749

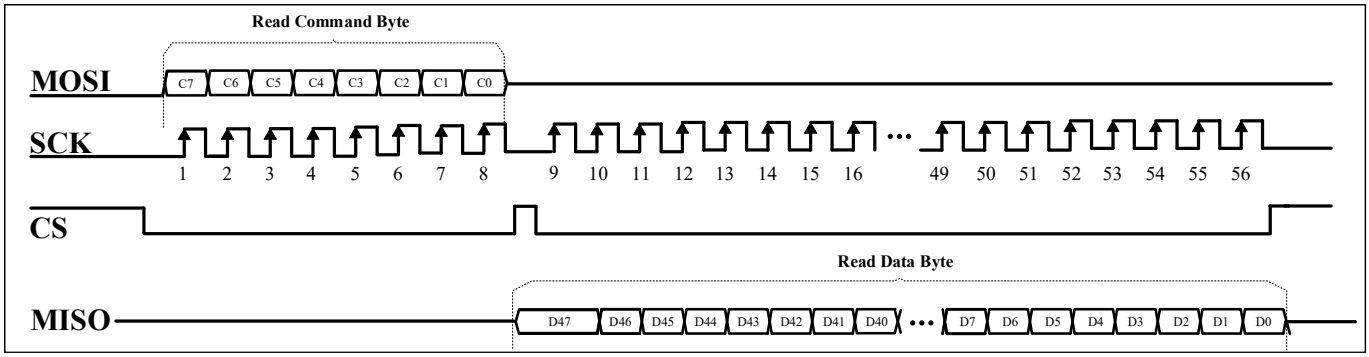


Figure 8 SPI Reading from IS32FL3749

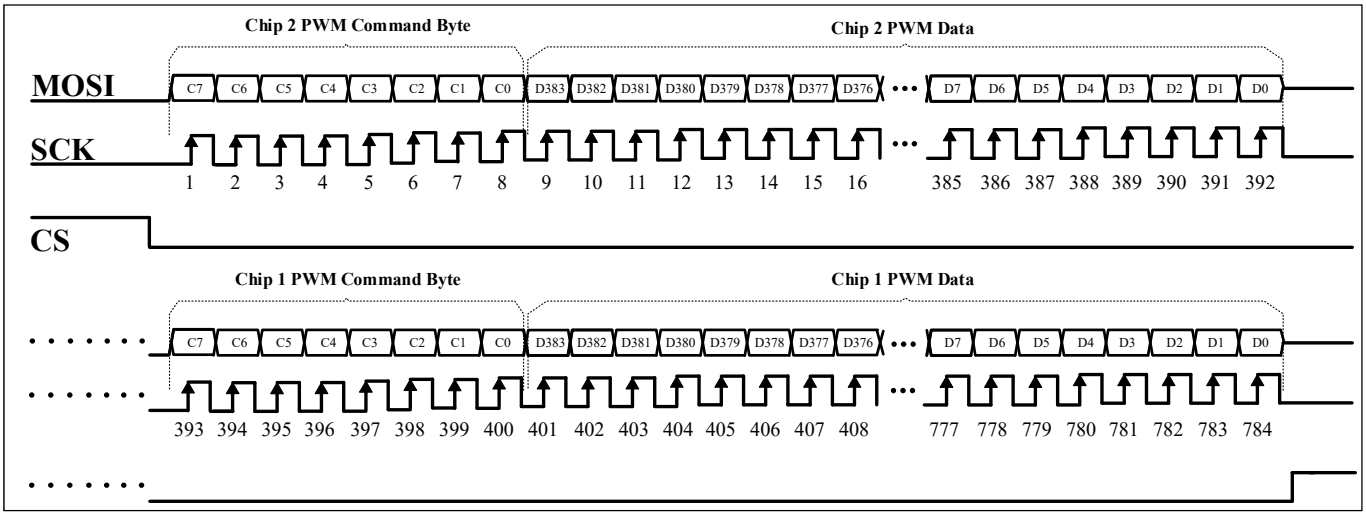


Figure 9 SPI Writing PWM Register Data to IS32FL3749 (Two Chips Cascade)

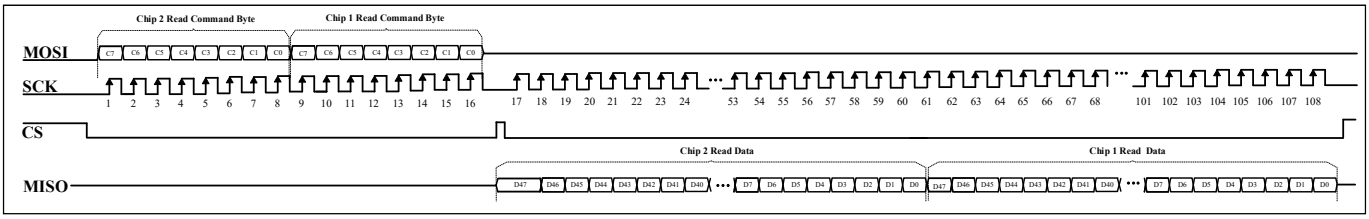


Figure 10 SPI Reading from IS32FL3749 (Two Chips Cascade)

VSB INTERFACE

IS32FL3749 uses a VSB protocol to control the chip's function with four wires: DI, SCLK, LAT and DO. VSB transfer starts from DI and SCLK controlled by Master (Microcontroller), and IS32FL3749 latches data when LAT is asserted (low to high).

The maximum SCLK frequency supported in IS32FL3749 is 33MHz.

WRITING OPERATION

VSB write data format is 8-bit (byte) command followed by the register data. The command byte determines the length and function of the register data. When writing Update/Reset/Fault Flag Clear Register to IS32FL3279, only the command is sent (without data). The IS32FL3749 VSB write register timing as shown in figure 12~15.

READING OPERATION

FC0, FC1, fault status, open/short detect result registers can be read by VSB.

To read the registers, the first command byte selects the corresponding register, followed by a LAT pulse to latch after read command byte is written to IS32FL3749. Read register timing as shown in figure 16/17/19/20, read the DI or DO data after sending the read command byte.

All register writes and read command as shown in Table 1.

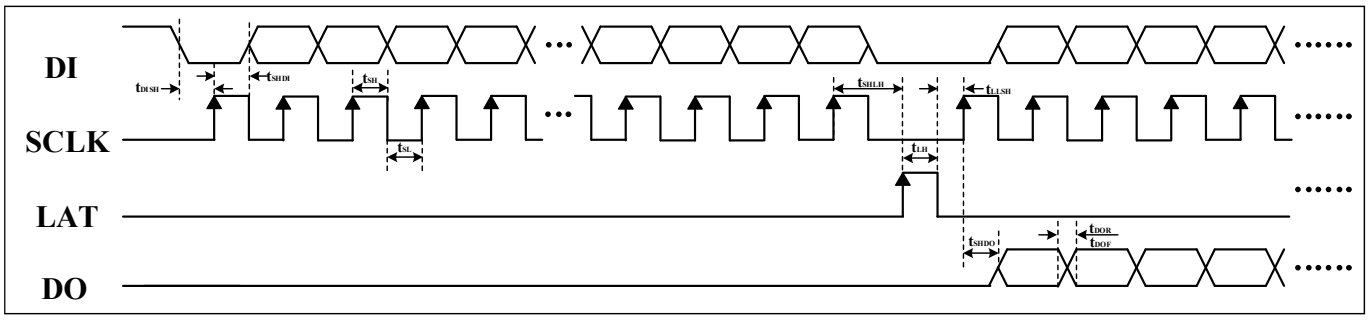


Figure 11 IS32FL3749 VSB Input Timing

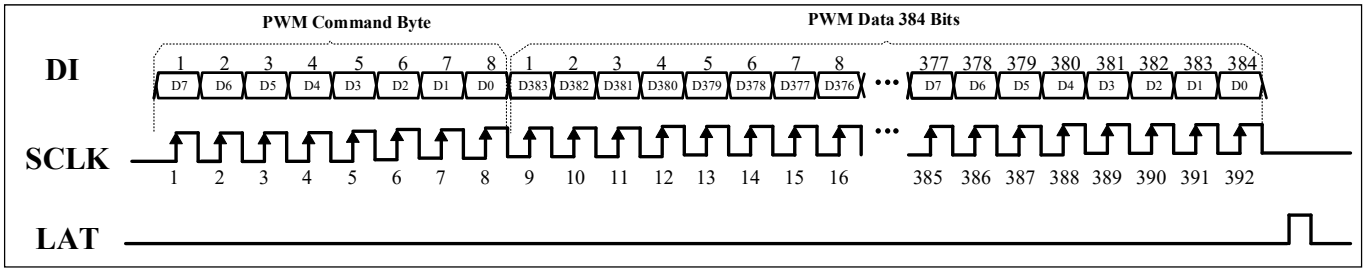


Figure 12 VSB Writing PWM Register Data to IS32FL3749

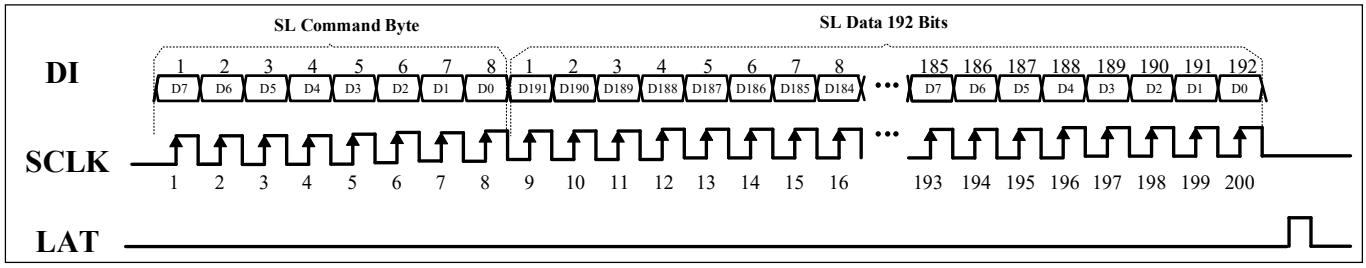


Figure 13 VSB Writing SL Register Data to IS32FL3749

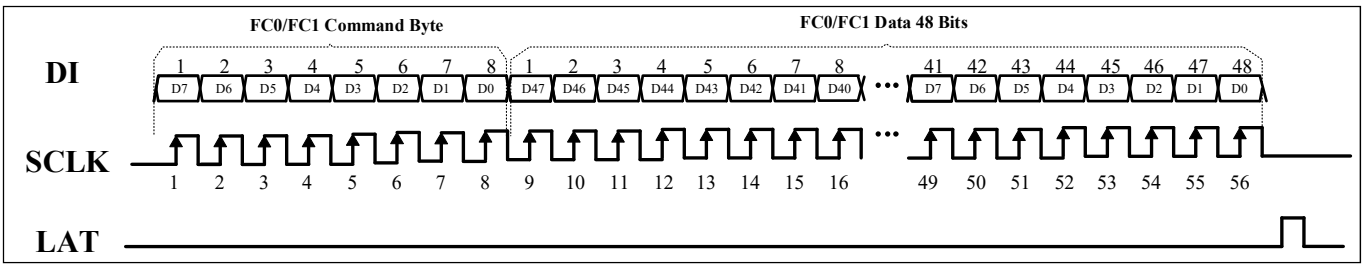


Figure 14 VSB Writing FCx Register Data to IS32FL3749

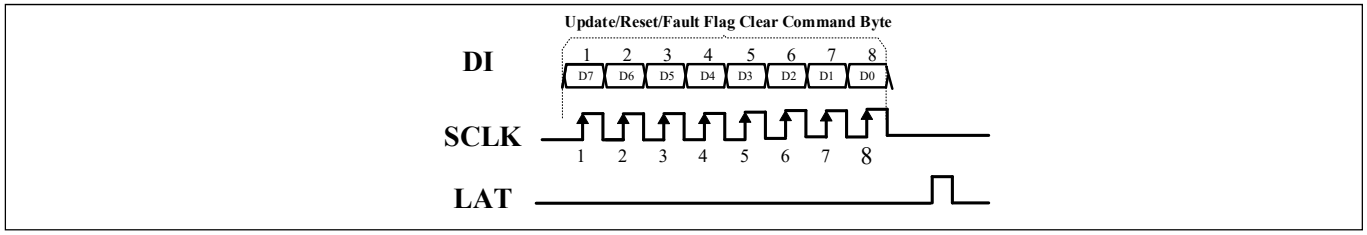


Figure 15 VSB Writing Update/Reset/Fault Flag Clear Register Data to IS32FL3749

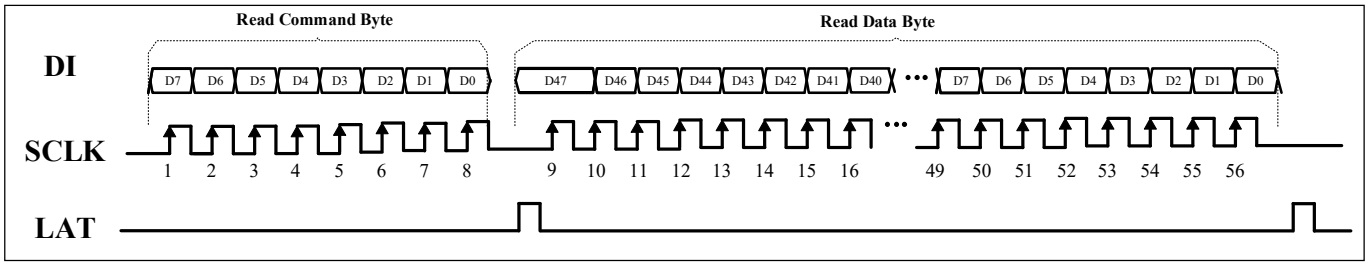


Figure 16 VSB Reading from IS32FL3749 (Bi-direction, read data from DI)

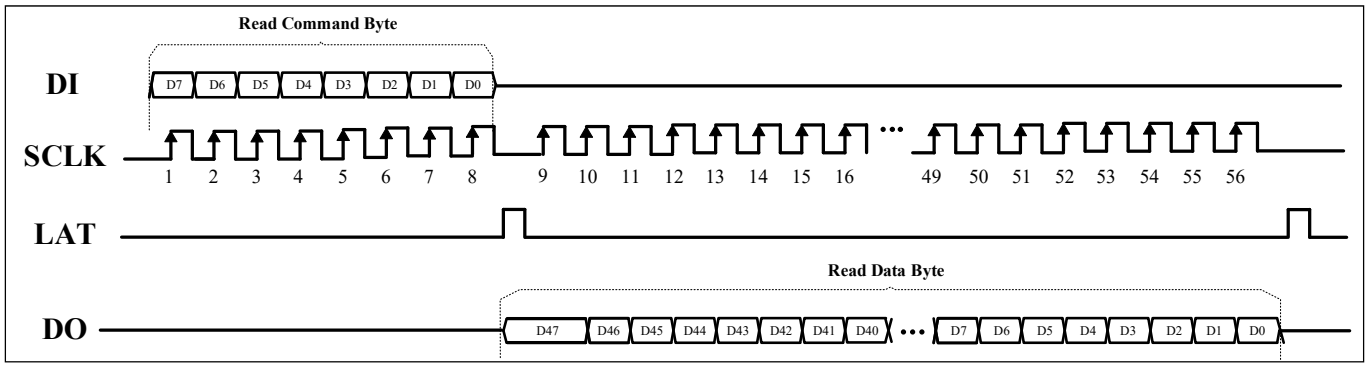


Figure 17 VSB Reading from IS32FL3749 (Single-direction, read data from DO)

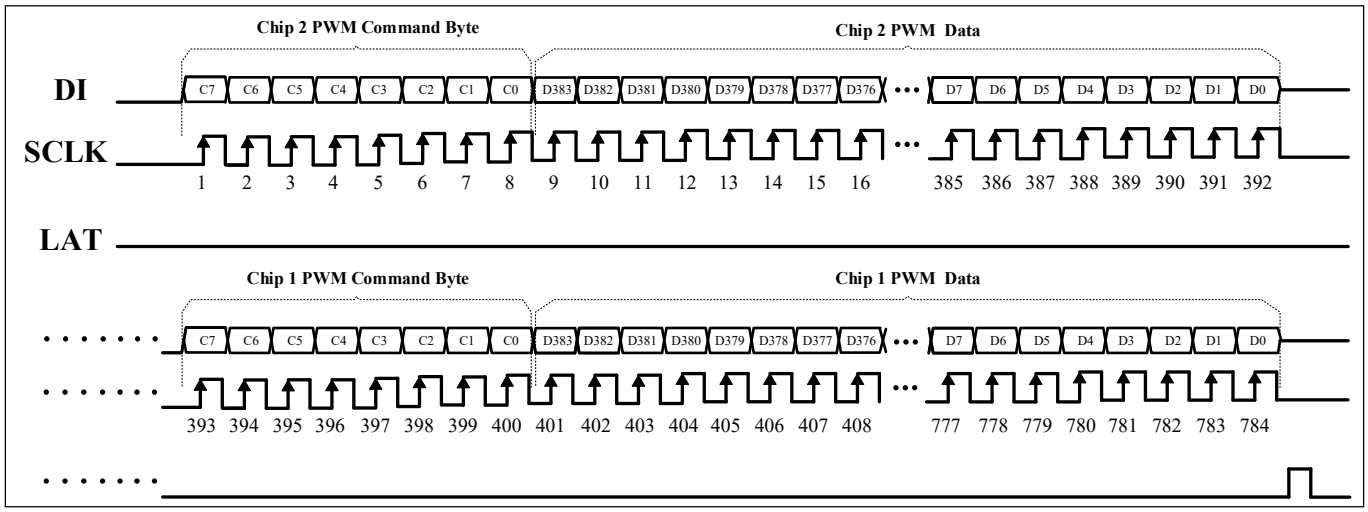


Figure 18 VSB Writing PWM Register Data to IS32FL3749 (Two Chips Cascade)

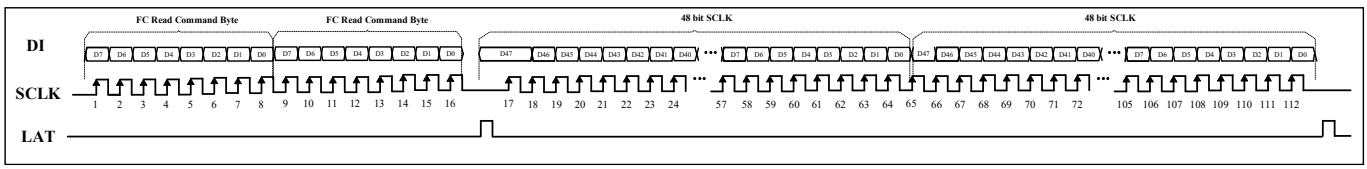


Figure 19 VSB Reading from IS32FL3749 (Two Chips Cascade, Bi-direction, read data from DI)

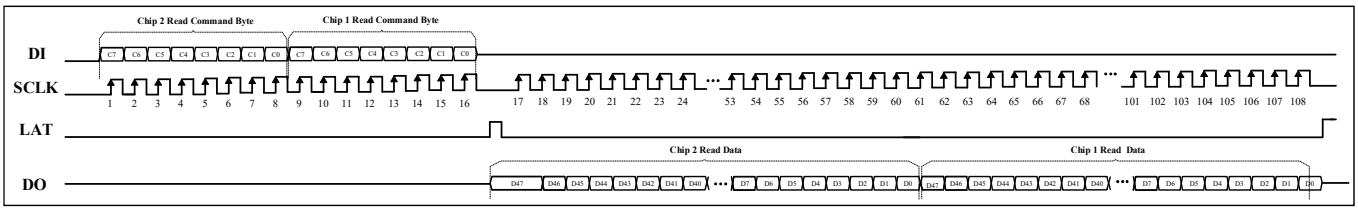


Figure 20 VSB Reading from IS32FL3749 (Two Chips Cascade Single-direction, read data from DO)

Table 1 Register Write and Read Command

Command	Data Length	Function
0110000x	8 bits+384 bits	Write PSW0 PWM Register data
0110001x	8 bits+384 bits	Write PSW1 PWM Register data
0110010x	8 bits+384 bits	Write PSW2 PWM Register data
0110011x	8 bits+384 bits	Write PSW3 PWM Register data
0100000x	8 bits+192 bits	Write PSW0 SL Register data
0100001x	8 bits+192 bits	Write PSW1 SL Register data
0100010x	8 bits+192 bits	Write PSW2 SL Register data
0100011x	8 bits+192 bits	Write PSW3 SL Register data
0010000x	8 bits+48 bits	Write FC0 Register data
1010000x	8 bits+48 bits	Read FC0 Register data
0010001x	8 bits+48 bits	Write FC1 Register data
1010001x	8 bits+48 bits	Read FC1 Register data
1011010x	8 bits+48 bits	Read open/short result of 24 channels
1101111x	8 bits+48 bits	Read fault flag status
0000001x	8 bits	Fault flag clear
0000100x	8 bits	Update PWM Register data
0000111x	8 bits	Global reset

REGISTER DEFINITION

Table 2 Register Definition

Unit	Name	Function	Table	R/W	Default
PWMx_0~PWMx_23	PWM Register	Set PWM for each LED	3	W	0000 0000 0000 0000
SLx_0~ SLx_23	Scaling Register	Set Scaling for each LED	4	W	1111 1111
FC0	Configuration Register	Configure operating mode	6	R/W	000000010
	Global Current Control Register	Set global current for R channels (CS0, CS3…CS21)	8	R/W	1111 1111
		Set global current for G channels (CS1, CS4…CS22)	9	R/W	1111 1111
		Set global current for B channels (CS2, CS5…CS23)	10	R/W	1111 1111
	Phase Delay & Edge select & Random enable Register	Set phase delay and select DI/DO edge and PSW random enable	11	R/W	01 1101
FC1	SYNC& Spread Spectrum	SYNC function and set spread spectrum	12	R/W	00 0000
	Temperature Status &GPWM Register	Set temperature thermal roll off and GPWM	13	R/W	00 0000
	De-ghost Time and PSW Pull down Voltage Selection Register	De ghost time and select Set the pull-down voltage for PSWx	14	R/W	000 0000
	CS Pull up Voltage Selection Register	Set the pull-up voltage for CSy	15	R/W	0000 0000
	Open/Short Detect and Open/Short Detest Threshold Register &PSMODE	LED open/short detection and set open/short detest threshold and power saving mode	16	R/W	0000 0000
	Read Direction Select Register	Set read direction	17	R/W	1
OS0~OS23	Open/Short Detect Result Register	Store the open/short information of LED	18	R	-
Fault Flag Status Read	Fault Flag Status Read Register	Store fault flag information	19	R	-
Fault Flag Clear	Fault Flag Clear Register	Fault flag clear	20	W	-
Update	PWM Update	Update PWM Register	21	W	-
Reset	Reset Register	Reset all registers	22	W	-

PWM Register

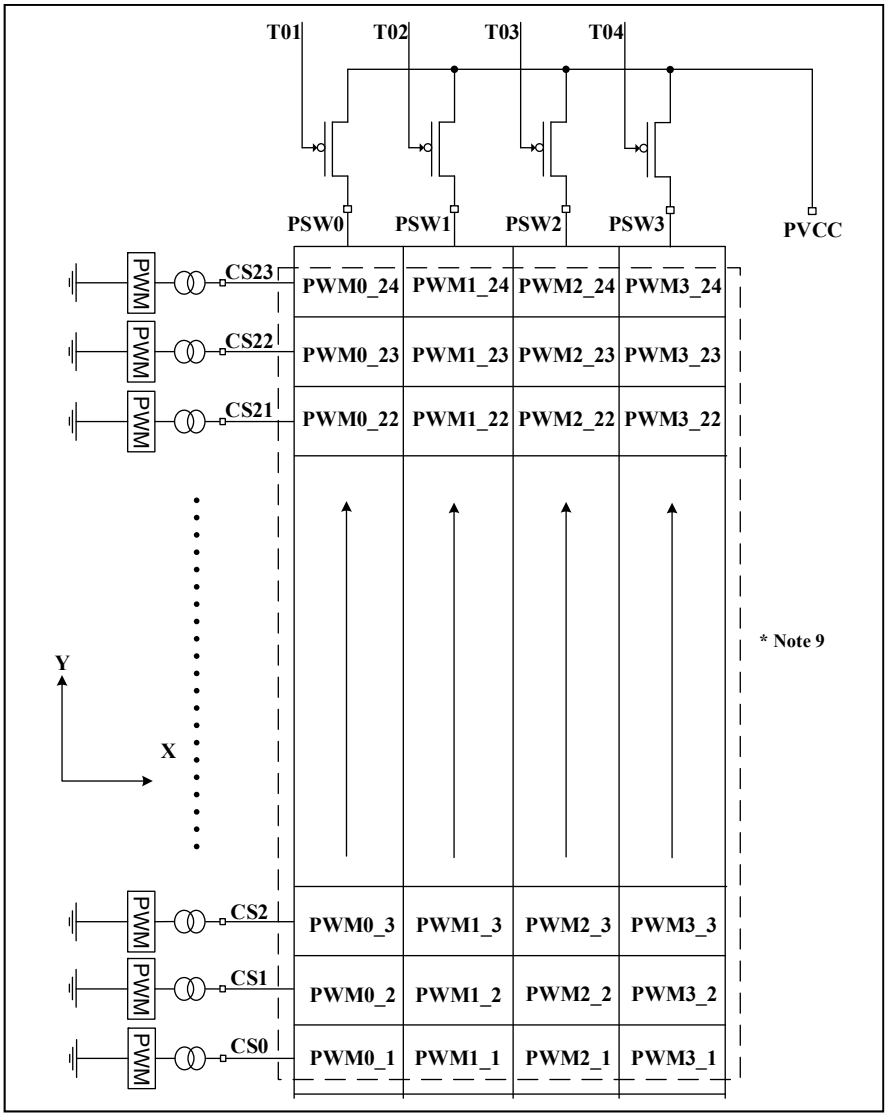


Figure 21 PWM Register

Note 9: PWMx_0~PWMx_23 is PWM Register for PSWx. Each PWMx_y contains 16-bit data, control the PWM duty of each dot. Each dot has two bytes PWM data to modulate the PWM duty in 256/4096/65536 steps.

Table 3 PWMx_0~PWMx_23 PWM Register

Unit	PWMx_23		…	PWMx_0	
Bit	383:376	375:368	…	15:8	7:0
Name	PWM_H	PWM_L	…	PWM_H	PWM_L
Default	00000000	00000000	…	00000000	00000000

Each dot has two PWM bytes to modulate the PWM duty in 256/4096/65536 steps. If using 8 bits PWM resolution, only PWM_H 8 bits need to be set. If using 8+4-bit PWM resolution, only PWM_H 8 bits and high 4 bits of PWM_L need to be set.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$ (8-bit mode)

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$ (8+4-bit mode)

N=65536: $PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$ (8+8bit/16-bit mode)

Where Duty is the duty cycle of PSWx, see SCANING TIMING section for more information. When PSWS= "000" and in 8+4-bit dithering/8+8-bit dithering/8bit PWM mode (OSC=16MHz), Duty is computed as below:

$$Duty = \frac{16.8\mu s}{(17.3\mu s + 0.3\mu s)} \times \frac{1}{4} = \frac{1}{4.19} \quad (2, 8\text{-bit mode})$$

When PSWS= "000" and in 16-bit PWM mode (OSC=16MHz), Duty is computed as below:

$$Duty = \frac{4.095ms}{(4.096ms + 0.0003ms)} \times \frac{1}{4} = \frac{1}{4.001} \quad (2,16\text{-bit mode})$$

I_{OUT} is the output current of CSy (y=0~23),

$$I_{OUT(PEAK)} = \frac{60}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

GCC is the Global Current Control register (D32:D9 of FC0) value, SL is the Scaling register value as Table 5 and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if in 8-bit PWM mode, PWM register D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=1kΩ, SL=1111 1111:

$$I_{LED} = \frac{60}{1k\Omega} \times \frac{255}{256} \times \frac{255}{256} \times \frac{1}{4.19} \times \frac{181}{256}$$

SL Register

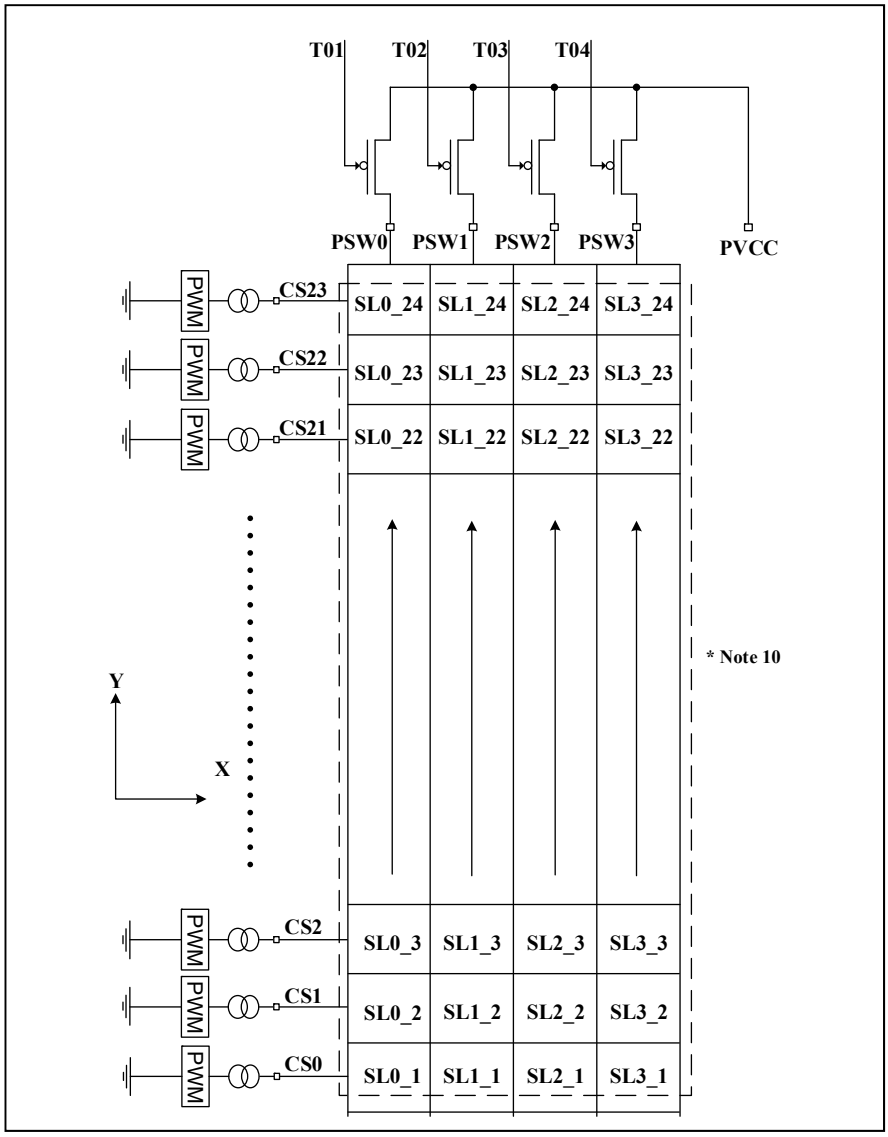


Figure 22 SL Register

Note 10: SLx_0~SLx_23 is SL Register for PSWx. Each SLx_y contains 8-bit data, control the DC output current of each dot. Each dot has a scaling byte to modulate the scaling in 256 steps.

Table 4 SLx_0~SLx_23 SL Register

Unit	SLx_23	…	SLx_1
Bit	191:184	…	7:0
Name	SL	…	SL
Default	11111111	…	11111111

Scaling register control the DC output current of each dot. Each dot has a scaling byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{60}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=0~23), GCC is the Global Current Control Register (D32:D9 of FC0) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if in 8-bit PWM mode, R_{ISET}=1kΩ, GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT} = \frac{60}{1k\Omega} \times \frac{255}{256} \times \frac{127}{256} = 29.6mA$$

$$I_{LED} = 29.6mA \times \frac{1}{4.19} \times \frac{PWM}{256}$$

Table 5 Function Register

Unit	Name	Function	Table	R/W	Default
FC0	Configuration Register	Configure operating mode	6	R/W	000000010
	Global Current Control Register	Set global current for R channels (CS0, CS3…CS21)	8	R/W	1111 1111
		Set global current for G channels (CS1, CS4…CS22)	9	R/W	1111 1111
		Set global current for B channels (CS2, CS5…CS23)	10	R/W	1111 1111
	Phase Delay & Edge select & Random enable Register	Set phase delay and select DI/DO edge and PSW random enable	11	R/W	01 1101
FC1	SYNC& Spread Spectrum	SYNC function and set spread spectrum	12	R/W	00 0000
	Temperature Status &GPWM Register	Set temperature thermal roll off and GPWM	13	R/W	00 0000
	De-ghost Time and PSW Pull down Voltage Selection Register	De ghost time and select Set the pull-down voltage for PSWx	14	R/W	000 0000
	CS Pull up Voltage Selection Register	Set the pull-up voltage for CSy	15	R/W	0000 0000
	Open/Short Detect and Open/Short Detest Threshold Register &PSMODE	LED open/short detection and set open/short detest threshold and power saving mode	16	R/W	0000 0000
	Read Direction Select Register	Set read direction	17	R/W	1
OS0~OS23	Open/Short Detect Result Register	Store the open/short information of LED	18	R	---- ----
Fault Flag Status Read	Fault Flag Status Read Register	Store fault flag information	19	R	---- ----
Fault Flag Clear	Fault Flag Clear Register	Fault flag clear	20	W	---- ----
Update	PWM Update	Update PWM Register	21	W	---- ----
Reset	Reset Register	Reset all registers	22	W	---- ----

Table 6 FC0 Unit (8:0) Configuration Register

Bit	8:6	5:3	2:1	0
Name	PSWS	OSC	PWMM	SSD
Default	000	000	01	0

The Configuration Register sets operating mode of IS32FL3749.

PSWS control the duty cycle of the PSW, default mode is 1/4.

The OSC bit selects the oscillator clock frequency, default is 16MHz.

The PWMM bit selects PWM resolution mode, default PWM resolution mode is 8+8-bit dithering.

When SSD is "1", IS32FL3749 enter software shutdown mode and to normal operate the SSD bit should set to "0".

PSWS PSW Scan Setting
000 PSW0~PSW3 scan
001 PSW0~PSW2 scan, PSW3 no active
010 PSW0~PSW1 scan, PSW2,3 no active
011 PSW0~PSW1 scan, PSW0=PSW2, PSW1=PSW3;
100 PSW0 scan only, PSW1,2,3 no active
101 PSW1 scan only, PSW0,2,3 no active
110 PSW2 scan only, PSW0,1,3 no active
111 PSW3 scan only, PSW0,1,2 no active

OSC Oscillator Clock Frequency Select
000 16MHz(default)
001 32MHz
010 8MHz
011 0.25MHz (only for 8-bit PWM mode)
100 12MHz
101 24MHz
110 6MHz
111 0.19MHz (only for 8-bit PWM mode)

PWMM PWM Mode Select
00 16-bit (OSC should be 24MHz or 32MHz)
01 8+8-bit dithering (OSC should be 24MHz or 32MHz)
10 8+4-bit dithering
11 8-bit

SSD Software Shutdown Control
0 Normal operation
1 Software shutdown

Table 7 PWM Frequency

PWM Frequency	32MHz	16MHz	8MHz	0.25MHz
16-bit	488Hz	-	-	-
8+8-bit	488Hz~ 125kHz	-	-	-
8+4-bit	7.8kHz~ 125kHz	3.9kHz~ 62.5kHz	1.95kHz~ 31.2kHz	-
8-bit	125kHz	62.5kHz	31.2kHz	0.97kHz

PWM Frequency	24MHz	12MHz	6MHz	0.19MHz
16-bit	366Hz	-	-	-
8+8-bit	366Hz~ 93.7kHz	-	-	-
8+4-bit	5.9kHz~ 93.7kHz	2.9kHz~ 46.8kHz	1.46kHz~ 23.4kHz	-
8-bit	93.7kHz	46.8kHz	23.4kHz	0.74kHz

Table 8 FC0 Unit (16:9) Global Current Control Register

Bit	16:9
Name	GCCR
Default	11111111

Set global current for R channels (CS0, CS3…CS21)

Table 9 FC0 Unit (24:17) Global Current Control Register

Bit	24:17
Name	GCCG
Default	11111111

Set global current for G channels (CS1, CS4…CS22)

Table 10 FC0 Unit (32:25) Global Current Control Register

Bit	32:25
Name	GCCB
Default	11111111

Set global current for B channels (CS2, CS5…CS23).
The Global Current Control Register modulates all CSy (y=0~23) DC current which is noted as I_{OUT} in 256 steps.
I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{60}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 11 FC0 Unit (38:33) Phase Delay & Edge Select & Random Enable Register

Bit	38	37:36	35	34	33
Name	RDMEN	TDO	DOE	DIE	PNR
Default	0	11	1	0	1

RDMEN control SW Random of scan enable bit. When RDMEN set to "1", PSW will pull up randomly and that is SW scan frequency will by random.

Set PNR to change the clock phase of odd channels and even channels. It is helpful for reduction power noise.

PDMEN PSW Random Scan
0 disable
1 enable

TDO DO Output Delay Time
00 0ns
10 1ns
01 2ns
11 3ns

DOE DO Transmit at SCK Edge
0 falling edge
1 rising edge

DIE DI Data Sample at SCK Edge
0 rising edge
1 falling edge

PNR Phase Delay
0 0-degree phase delay
1 180-degree phase delay

Table 12 FC1 Unit (6:0) SYNC& Spread Spectrum Register

Bit	6	5:4	3:2	1:0
Name	SSP	-	SCLT	MS
Default	0	00	00	00

Spread Spectrum Register set the spread spectrum (SSP) and synchronization function of IS32FL3749. The spread spectrum range is ±5%. When SSP enable, the spread spectrum function will be enabled and the SCLT bits will adjust the cycle time of spread spectrum function. The oscillator clock frequency recommends that the 8MHz be at least when the spread spectrum function is enabled.

When two or more IS32FL3749 are cascaded, the MS bit is set to "11" for the master IS32FL3749. The master IS32FL3749's SYNC/GCLK pin will generate a clock signal to all the slave devices. To be configured as a clock slave device and accept an external clock input the slave device's MS bit must be set to "10".

SSP Spread Spectrum Function Enable
0 disable
1 enable

SCLT Spread Spectrum Cycle Time
00 1980μs
01 1200μs

MS Enable of SYNC Function
0x Disable, 30kΩ pull-down (default)
10 slave mode
11 master mode

Table 13 FC1 Unit (13:7) Temperature Status &GPWM Register

Bit	13:12	11:10	9:8	7
Name	GPWM	TS	TROF	TSD
Default	00	00	00	1

TS store the temperature point of the IC. If the IC temperature reaches the temperature point the IC will trigger the thermal roll off and will decrease the current as TROF set percentage.

When TSD are set to "0", the thermal shutdown function enables. If environment temperature higher than maximum safe working temperature, IS32FL3749 will work in shutdown mode automatically, and it will go back in normal operation when the temperature drops.

GWPM Global PWM Control
0x function off, follow PWM controller
10 all channels' PWM=0
11 all channels' PWM=100%

TS Thermal Roll Off Start Point
00 140°C
01 120°C
10 100°C
11 90°C

TROF Percentage of Output Current
00 100%
01 75%
10 55%
11 30%

TSD Thermal Shutdown
0 disable
1 enable

Table 14 FC1 Unit (19:14) De-ghost Time and PSW Pull down Voltage Selection Register

Bit	19:18	17	16:14
Name	DTS	PSWTS	PSWPD
Default	00	0	000

Set DTS to select PSW interval de-ghost time.

Set PSWTS to select PSW pull down during off time or de-ghost time.

Set PSWPD to select pull down voltage for PSW.

DTS PSW Interval De-ghost Time (OSC=16MHz)
00 5 PWM clock cycle(default)
01 12 PWM clock cycle
10 30 PWM clock cycle
11 Not allowed

PSWTS PSW Pull down Time Select
0 PSW pull down during off time
1 PSW pull down during de-ghost time

PSWPD PSW De-ghost Pull down Voltage
000 floating (default)
001 0V
010 1.4V
011 2.1V
100 2.8V
101 3.5V
110 4.2V
111 5.6V

Table 15 FC1 Unit (27:20) CS Pull up Voltage Selection Register

Bit	27:24	23:20
Name	CSGBPU	CSRPU
Default	0000	0000

Set CSRPU to select pull up voltage for R group channels (CS0, CS3…CS21).

Set CSGBPU to select pull up voltage for G group channels and B group channels (CS1&CS2, CS4&CS5…CS22&CS23).

CSGBPU G&B Group Pull up Voltage
0000 floating (default)
0001 PV_{CC}-10.8V
0010 PV_{CC}-10.1V
0011 PV_{CC}-9.4V
0100 PV_{CC}-8.7V
0101 PV_{CC}-8.0V
0110 PV_{CC}-7.3V
0111 PV_{CC}-6.6V
1000 PV_{CC}-5.9V
1001 PV_{CC}-5.2V
1010 PV_{CC}-4.5V
1011 PV_{CC}-3.8V
1100 PV_{CC}-3.1V
1101 PV_{CC}-2.4V
1110 PV_{CC}-1.7V
1111 PV_{CC}-1V

CSRPU R Group Pull up Voltage
0000 floating (default)
0001 PV_{CC}-10.8V
0010 PV_{CC}-10.1V
0011 PV_{CC}-9.4V
0100 PV_{CC}-8.7V
0101 PV_{CC}-8.0V
0110 PV_{CC}-7.3V
0111 PV_{CC}-6.6V
1000 PV_{CC}-5.9V
1001 PV_{CC}-5.2V
1010 PV_{CC}-4.5V
1011 PV_{CC}-3.8V
1100 PV_{CC}-3.1V
1101 PV_{CC}-2.4V
1110 PV_{CC}-1.7V
1111 PV_{CC}-1V

Table 16 FC1 Unit (38:28) Open/Short Detect and Open/Short Detect Threshold Register &PSM Register

Bit	38:37	36:35	34:33	32:31	30:29	28
Name	OSDE	OSDS	-	SDRNT	ODRNT	PSM
Default	00	00	00	00	00	0

OSDE enables the open or short LED channel detection with the result stored in open/short detect result register, note either open or short information is saved not both.

Set OSDS to select open or short detect PSWx.

Power Saving Mode (PSM) allows IS32FL3749 enter low power consumption status. After entering this mode, can reduce quiescent power supply current, and the output current of each channel only support 1/3.5 maximum output current (typical value, example: 17mA when R_{ISET}=1.0kΩ).

OSDE Open/Short Detect
0x disable
10 Short detect
11 Open detect

OSDS Open/Short Detect Scanline Select
00 PSW0 open/short detect
01 PSW1 open/short detect
10 PSW2 open/short detect
11 PSW3 open/short detect

SDRNT Short Select Threshold Select
00 (PV_{CC}×0.925) V (default)
01 (PV_{CC}×0.943) V
10 (PV_{CC}×0.962) V
11 (PV_{CC}×0.907) V

ODRNT Open Detect Threshold Select
00 0.15V (default)
01 0.2V
10 0.25V
11 0.1V

PSM Power Saving Mode
0 disable
1 enable

Table 17 FC1 Unit (47) Read Direction Select Register

Bit	47
Name	SIOM
Default	1

Set SIOM to select read data mode.

IS32FL3749 support single direction and Bi-direction to reading data when uses VSB (Video serial bus) interface.

When select read data single direction, read register data from DO pin after sending the read command.

When select Read data Bi-direction, read register data from DI pin after sending the read command.

SIOM Read Direction Select
0 Read data Bi-direction
1 Read data single direction

Table 18 OS23~OS0 Unit (23:0) Open/Short Detect Result Register (Read Only)

Bit	23:0
Name	OS23:OS0
Default	-

When OSDE (D38:D37 of FC1) is set to “11”, open detection will enable, and the LED open status will be detected in real time, the open information will be stored at this register.

When OSDE (D38:D37 of FC1) is set to “10”, short detection will enable, and the LED short status will be detected in real time, the short information will be stored at this register.

Before set OSDE, the GCC should set to 0x0F, and need send Fault Flag Clear each time before reading open detect result or short detect result.

Please check OPEN/SHORT DETECT FUNCTION section for more information.

Table 19 Fault Flag Read (DEh) Unit (7:0) Fault Flag Status Read Register (Read Only)

Bit	7	6	5	4	3	2	1	0
Name	P3OC	P2OC	P1OC	P0OC	SF	OF	TSF	RSF
Default	0	0	0	0	0	0	0	0

P3OC PSW3 Over Current Flag
0 normal
1 over current

P2OC PSW2 Over Current Flag
0 normal
1 over current

P1OC PSW1 Over Current Flag
0 normal
1 over current

P0OC PSW0 Over Current Flag
0 normal
1 over current

SF Short Flag
0 normal
1 LED short

OF Open Flag
0 normal
1 LED open

TSF Thermal Shutdown Flag
0 normal
1 thermal shutdown

RSF ISET Pin Short to Ground Flag
0 normal
1 ISET pin short to GND

Table 20 Fault Flag Clear Unit (7:0) Register (Write Only)

Bit	7:0
Name	Fault Flag Clear
Default	-

When SDB= “H” and SSD= “1”, send Fault Flag Clear Command(0x02) to IS32FL3749 will clear Fault Flag Register status and Open/Short detect result Register status.

Table 21 PWM Update Unit (7:0) Register (Write Only)

Bit	7:0
Name	Update
Default	-

When SDB= “H” and SSD= “0”, send Update Command(0x08) to IS32FL3749 will update the PWM register (PWMx_0~PWMx_23) values.

Table 22 Reset Unit (7:0) Reset Register (Write Only)

Bit	7:0
Name	Reset
Default	-

When working in normal operation mode, sending Reset Command (0x0E) to IS32FL3749 will reset all registers to default values.

APPLICATION INFORMATION

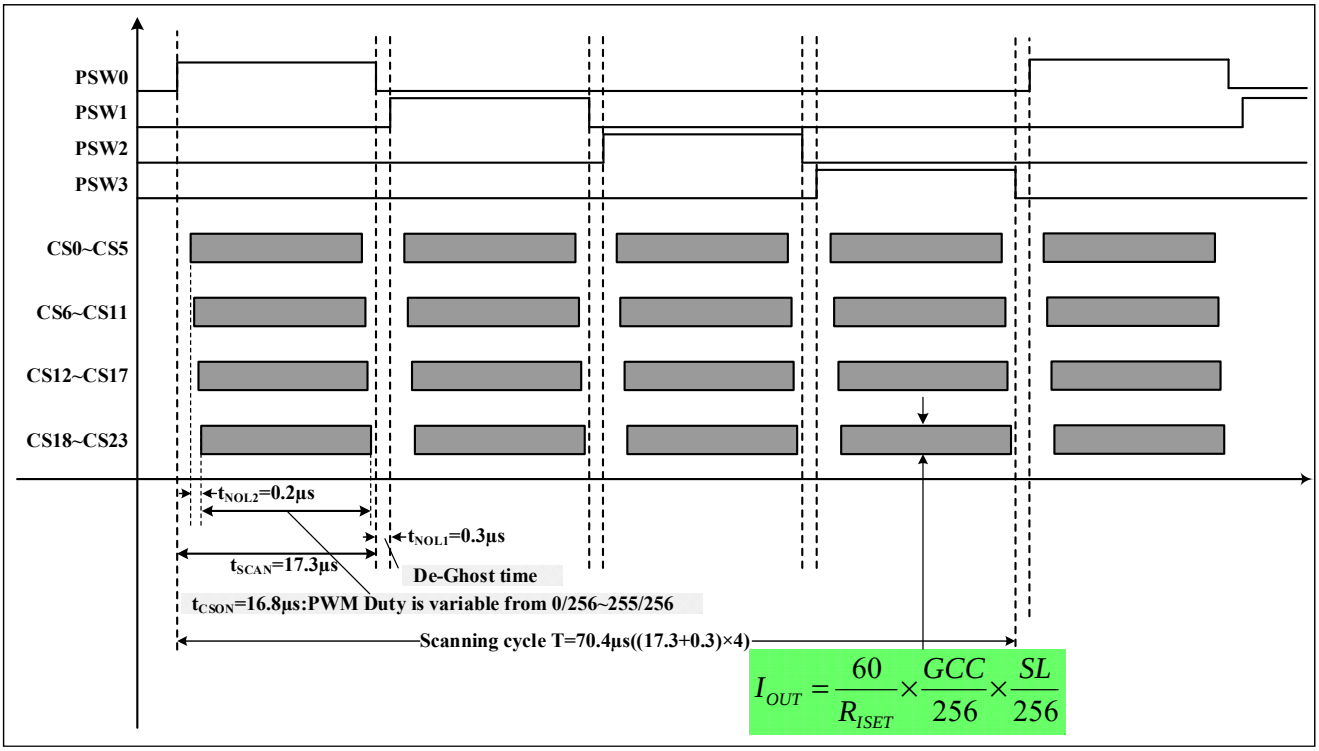


Figure 23 Scanning Timing (8-bit PWM Mode, OSC=16MHz)

SCANING TIMING

As shown in Figure 23, the PSW0~PSW3 is turned on by serial, LED is driven 4 by 4 within the PSWx (x= 0~3) on time (PSWx, x= 0~3 is source and it is high when LED on) and in 8+4-bit dithering/8+8-bit dithering/8bits PWM mode (OSC=16MHz), including the non-overlap blanking time during scan, the duty cycle of PSWx (active high, x= 0~3, PSWS= "000") is:

$$Duty=\frac{16.8\mu s}{(17.3\mu s+0.3\mu s)}\times\frac{1}{4}=\frac{1}{4.19} \qquad (2)$$

Where 16.4μs is t_{SCAN}, the period of PSWx scanning, 15.9μs is t_{CSON}, the CS-ON time during scan,0.3μs is t_{NOL1}, the non-overlap time.

PWM CONTROL

After setting the I_{OUT}, GCC and SL, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register in 8bits PWM mode (OSC=16MHz).

For PSWS= "000", I_{OUT} is computed by the Formula (2):

$$Duty=\frac{16.8\mu s}{(17.3\mu s+0.3\mu s)}\times\frac{1}{4}=\frac{1}{4.19} \qquad (2)$$

$$GCC=\sum_{n=0}^{7}D[n]\cdot 2^n$$

$$SL=\sum_{n=0}^{7}D[n]\cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

The value of the PWM Registers decides the average current of each LED noted I_{LED}, I_{LED} is computed as Formula (1):

$$I_{LED}=\frac{PWM}{N}\times I_{OUT(PEAK)}\times Duty \qquad (1)$$

$$PWM=\sum_{n=0}^{7}D[n]\cdot 2^n$$

Where PWM is PWM Registers data showing in Table 4.

For example, if in 8-bit PWM mode, R_{ISET}= 1kΩ, PWM= 255, and GCC= 255, SL= 255, then

$$I_{OUT(PEAK)}=\frac{60}{1k\Omega}\times\frac{255}{256}\times\frac{255}{256}=59.5mA$$

$$I_{LED}=I_{OUT(PEAK)}\times\frac{1}{4.19}\times\frac{PWM}{256}$$

OPERATING MODE

IS32FL3749 can only operate in PWM Mode. The brightness of each LED can be modulated with 256/4096/65536 steps by PWM registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS32FL3749 has open/short detect bit for each LED.

The open/short status register stores the open/short information of LED string.

To get the correct open/short information, several configurations are recommended to set before setting the OSDE bit (D38:D37 of FC1):

The two configurations need to set before setting the

OSDE bits:

1 0x0F≤GCC≤0x40

2 PSWx Pull Down Voltage = floating,

CSy Pull Up Voltage = floating,

3 PWM >40%

Where GCC is the Global Current Control Register and the Pull down/up Voltage Selection Register set (D16:D14 of FC1) to 0x000 is set PSWx pull-down voltage and (D23:D20/D27:D24 of FC1) set to 0x0000 is set CSy pull-up voltage to floating.

The detect action is one-off event and each time before reading out the open/short information need clear Fault Flag Register status (send Fault Flag Clear Command(0x02)).

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS32FL3749 has integrated Pull down voltage setting for each PSWx (x=0~3) and Pull up voltage setting for each CSy (y=0~23). Select the right PSWx Pull down voltage (D16:D14 of FC1) and CSy Pull up voltage (D27:D20 of FC1) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, need to depending on how many LED is connect in series in one LED dot position, selecting the voltage setting will be sufficient to eliminate the LED ghost phenomenon.

When IS32FL3749 works in shutdown mode, the de-ghost function should be disabled.

PHASE DELAY AND GROUP DELAY

Phase Delay

IS32FL3749 support change the clock phase of adjacent channels, it is helpful for reduction power noise.

When phase delay is enabled, the CS0/2/4…22 channels is start from left, and CS1/3/5…23 channels start from right, the CSy timing as illustrated in Figure 24:

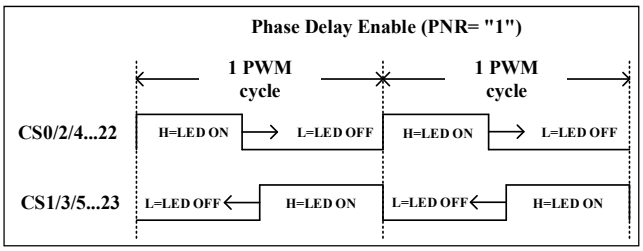


Figure 24 CSy Timing (Phase Delay Enable)

When phase delay is disabled, all channels are start from left together, the CSy timing as illustrated in Figure 25:

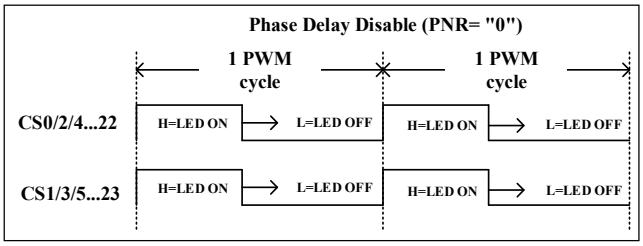


Figure 25 CSy Timing (Phase Delay Disable)

Group Delay

IS32FL3749 divide all CS channels into 4 groups, set 4 groups delay to minimize the power ripple and one PWM clock delay for each group to reduce transient noise. The groups delay as illustrated in Figure 26:

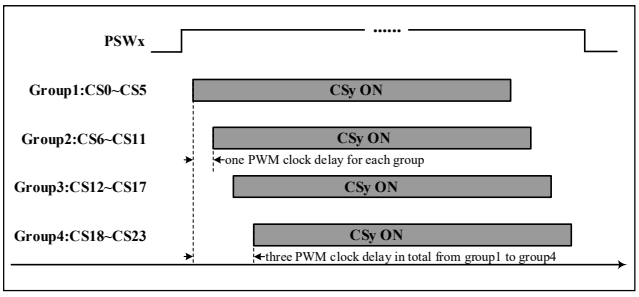


Figure 26 CSy Group DelayTiming

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (D0 of FC0) to “1”, the IS32FL3749 will operate in software shutdown mode. When the IS32FL3749 is in

software shutdown, all current sinks are switched off, so that the matrix is blanked.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS32FL3749 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks' supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 10μF + 0.1μF capacitor for PVCC pin, if possible, with a 0.47μF or 1μF capacitor is recommended to connected to the ground at each power supply pins of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

1. The V_{CC} (PVCC, VCC) capacitors need to close to the chip and the ground side should well have connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side's ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

4. The CSy pins maximum current is 60mA (R_{ISET}=1kΩ), and the PSWx pins maximum current is larger, the width of the trace, PSWx should have wider trace then CSy.

THERMAL CONSIDERATION

The over temperature of the chip may result in deterioration of the properties of the chip. IS32FL3749 has thermal pad but the chip could be very hot if power is very large. So, do consider the ground area connects to the GND pins and thermal pad. Other traces should keep away and ensure the ground area below the package is integrated, and the back layer should be connected to the thermal pad thru 9 or 16 vias to be maximized the area size of ground plane.

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (4):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (4)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{38.9°C/W} \approx 2.57W$$

Figure 27, shows the power derating of the IS32FL3749 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

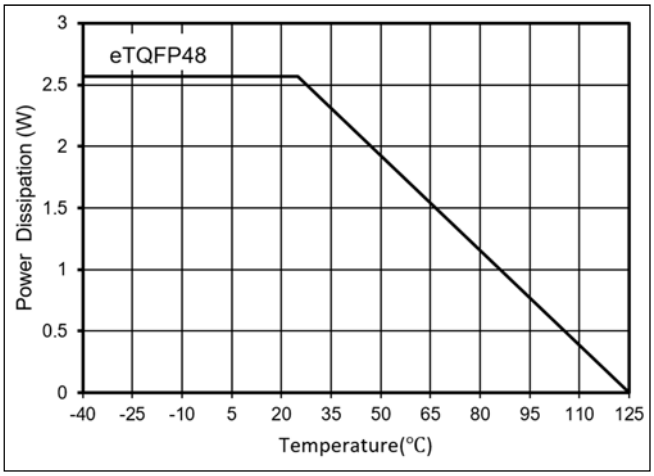


Figure 27 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

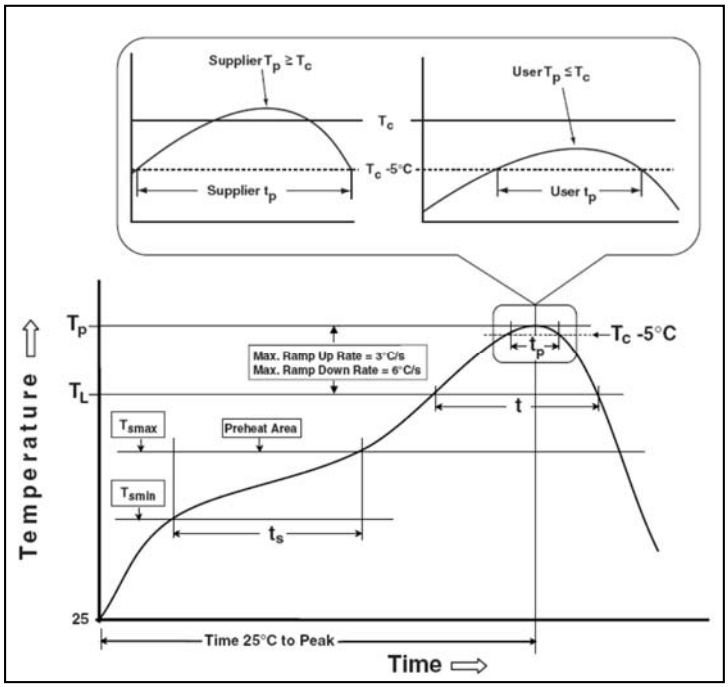
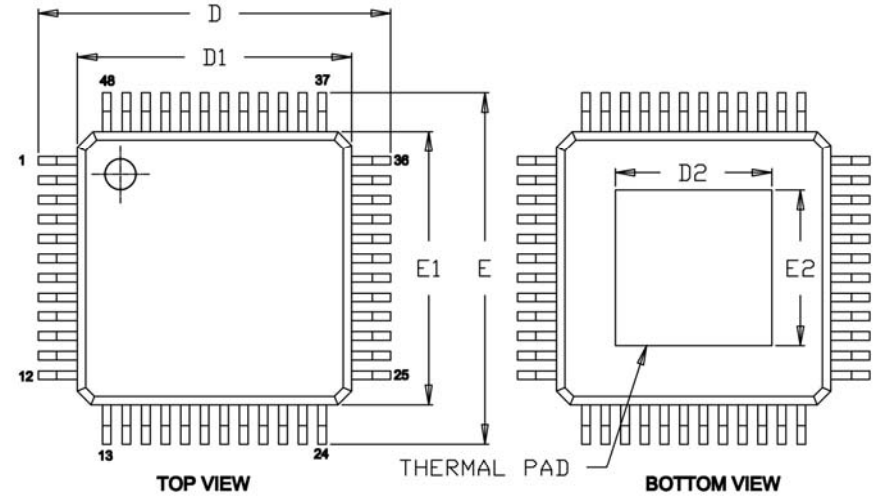
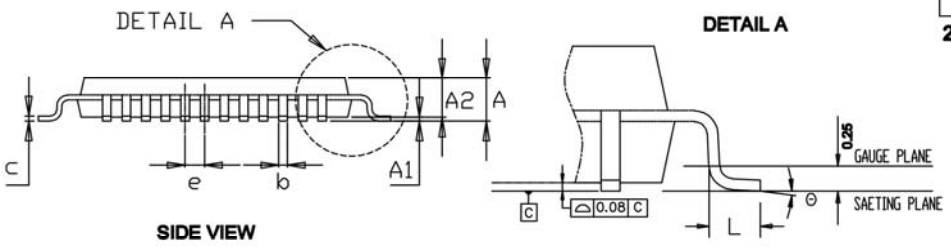


Figure 28 Classification profile

PACKAGE INFORMATION

eTQFP-48





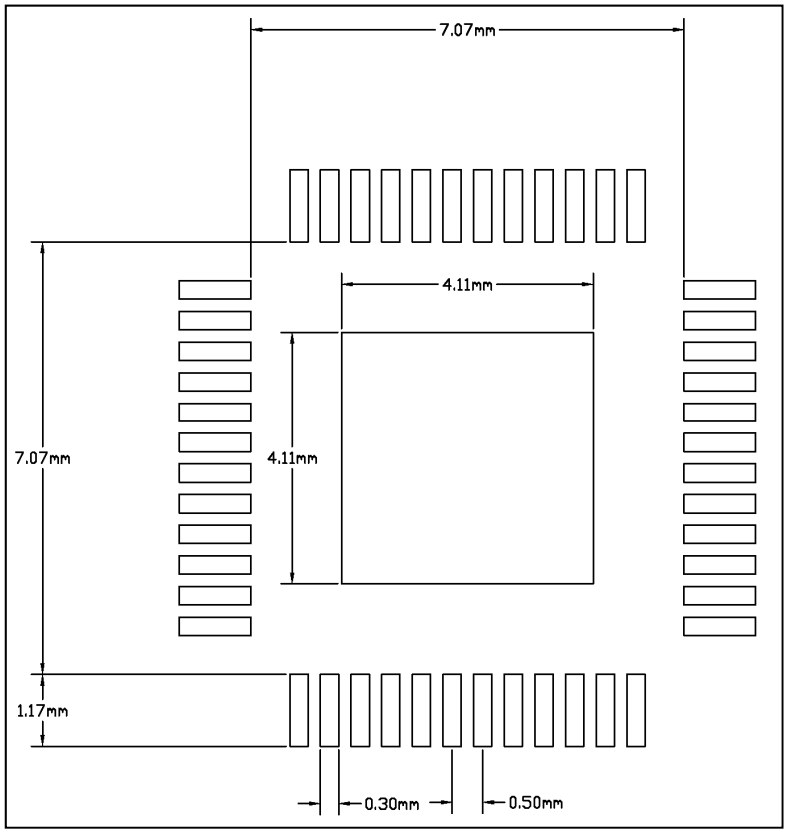
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D		9.00 BSC	
D1		7.00 BSC	
D2	4.00	—	4.21
E		9.00 BSC	
E1		7.00 BSC	
E2	4.00	—	4.21
L	0.45	0.60	0.75
b	0.17	0.22	0.27
e		0.50 BSC	
c	0.09	—	0.20
θ	0°	—	7°

233-570-252 Rev. B

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

eTQFP-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2022.02.23
0B	1.Update application circuit (cascade Figure2/3) 2.Update DIGITAL INPUT SWITCHING CHARACTERISTICS 3.Update VSB INTERFACE description 4.Update SPI/VSB Input timing (Figure4/12) and add cascade write/read timing	2022.09.13
0C	1. Add PWM Frequency (Table 8) 2. Update MISO/DO Transmit Edge (DOE at Table12 (D35 of FC1)) 3. Update Read Direction Select (SIOM at Table18 (D47 of FC1)) 4. Update EC table 5. Add phase delay description at APPLICATION INFORMATION	2023.09.08
A	Update to final version	2023.12.19
B	Add IS32FL3749-TQLCA3-TR part number in ordering information	2024.07.03