IS32FL3248

48-CHANNEL, 16-BIT PWM LED DRIVER

March 2024

GENERAL DESCRIPTIONS

The IS32FL3248 is a 48-channel constant current LED driver. Each channel has 16-bit PWM brightness control, and 64 steps of constant-current scaling (SL). SL can adjust brightness deviation between channels. GCC can adjusts brightness deviation between the R, G, and B color groups. The 8 steps maximum current band control (CB) selects the maximum output current range for all channels.

Proprietary programmable algorithms are used in IS32FL3248 to minimize audible noise that can result from MLCC decoupling capacitor. SL, GCC, CB and all other registers can be programmed via a high-speed VSB (video series bus, up to 25MHz) or SPI (up to 25MHz) serial interface port.

IS32FL3248 software shutdown mode can put the device to sleep (for minimum power consumption) while retaining all register values.

IS32FL3248 is available in eLQFP-64 (10mm×10mm) and WFQFN-64 (9mm×9mm) packages. It operates from 3.0V to 5.5V over the temperature range of -40°C to +125°C.

APPLICATIONS

- Mini LED Back Light
- Automotive LED Back Light
- Automotive Center Information Display
- Automotive Signage
- LED Video Displays

FEATURES

- V_{CC}= 3.0V to 5.5V
- 48 current sink output channels tolerate up to 16V, multiple LEDs can be connected in series
- Support 48 current sink output channels and sink current capability with CB and GCC
  - 33.8mA (V_{CC}≥ 3.6V, CB= “111”,)
  - 24.8mA (V_{CC}< 3.6V, CB= “101”,)
- Maximum Current Band (CB)
  - 3-bit (8 steps) with a 9.7% to 100% range
- DC Current Scaling (SL)
  - 6-bit (64 steps) with a 25.9% to 100% range
- Individual 16-bit, 8+8-bit dithering, 8+4-bit dithering, 8-bit PWM mode
- Global Current Control (GCC)
  - 8-bit (256 steps) with a 9.6% to 100% range
  - 3 GCC sets for each color group
- Constant Current Accuracy
  - Channel to Channel= ±3% (Max.@25°C)
  - Channel to Channel= ±5% (Max.@-40°C~125°C)
  - Device to Device= ±3% (Max.@25°C)
  - Device to Device= ±6% (Max.@-40°C~125°C)
- Chain topology via VSB interface, PWM data I/O is daisy chained with bi-directional data transmission (write and read)
- Support bi-directional data output via DI
- Display timing reset
- Real-time LED open detection (LOD)
- Real-time LED short detection (LSD)
- Over temperature protection
- Spread spectrums
- Software shutdown mode
- 180-degree phase delay operation to reduce power noise
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- eLQFP-64 (10mm×10mm) and WFQFN-64 (9mm×9mm) packages
- RoHS & Halogen-Free Compliance
- TSCA Compliance

TYPICAL APLICATION CIRCUITE

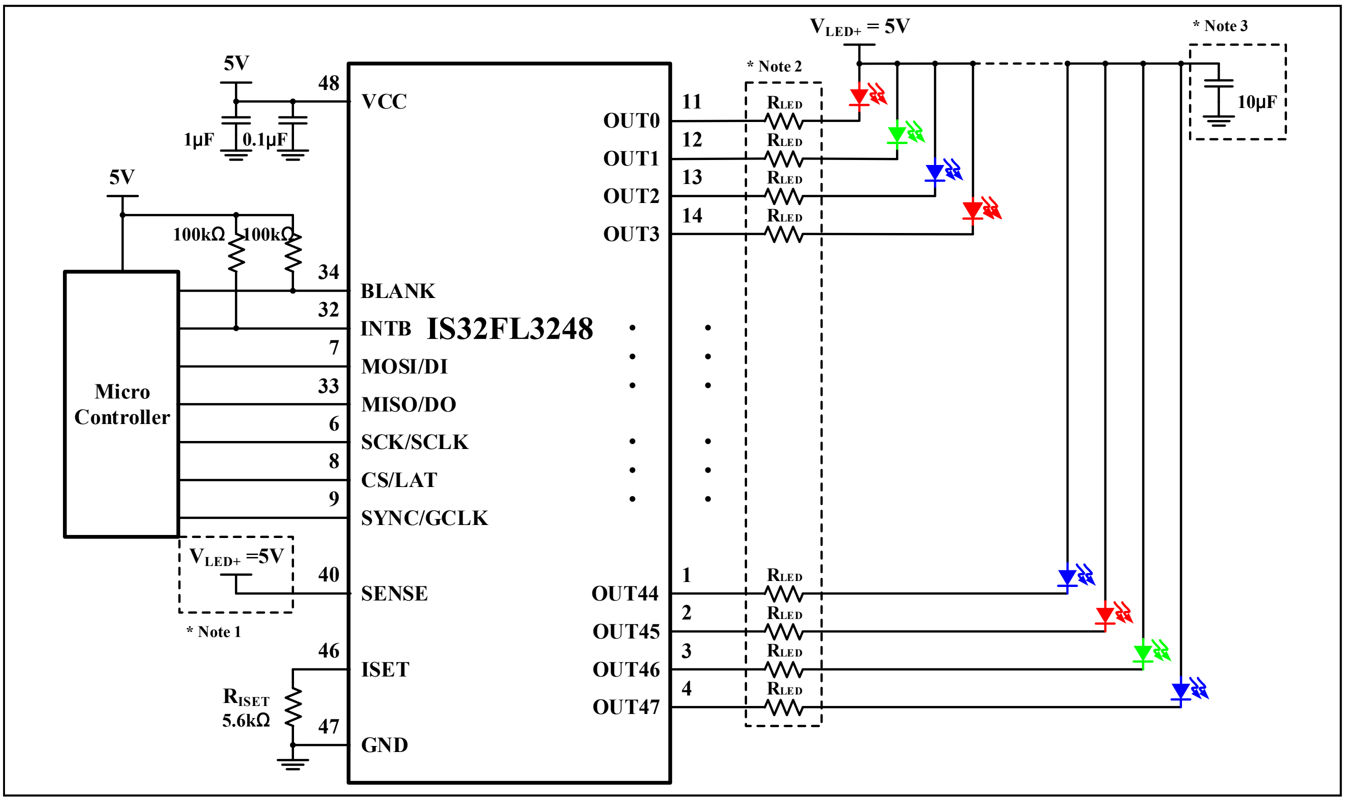


Figure 1 Typical Application Circuit

TYPICAL APLICATION CIRCUITE (CONTINUED)

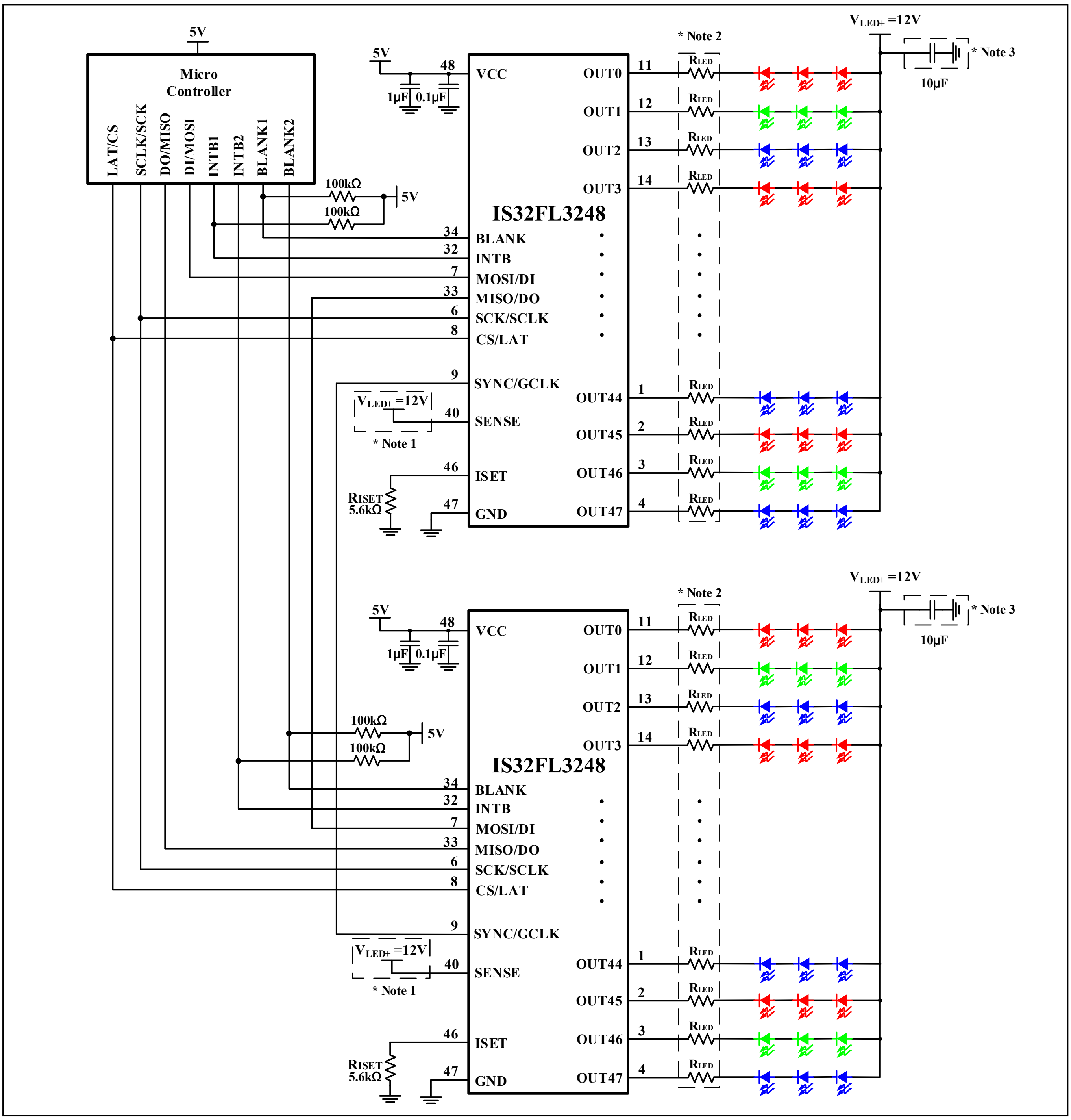


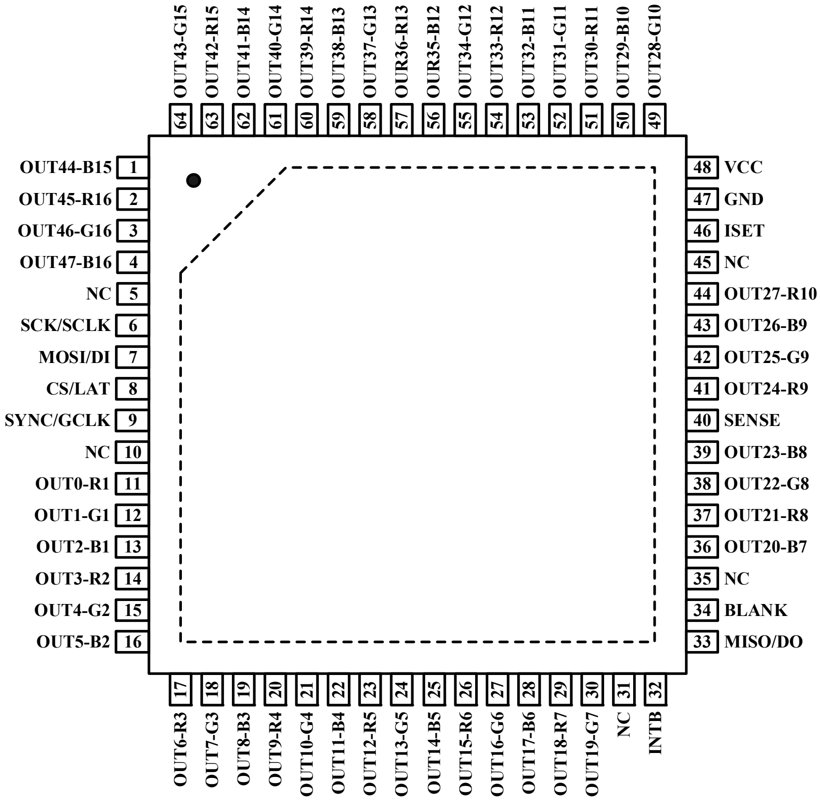
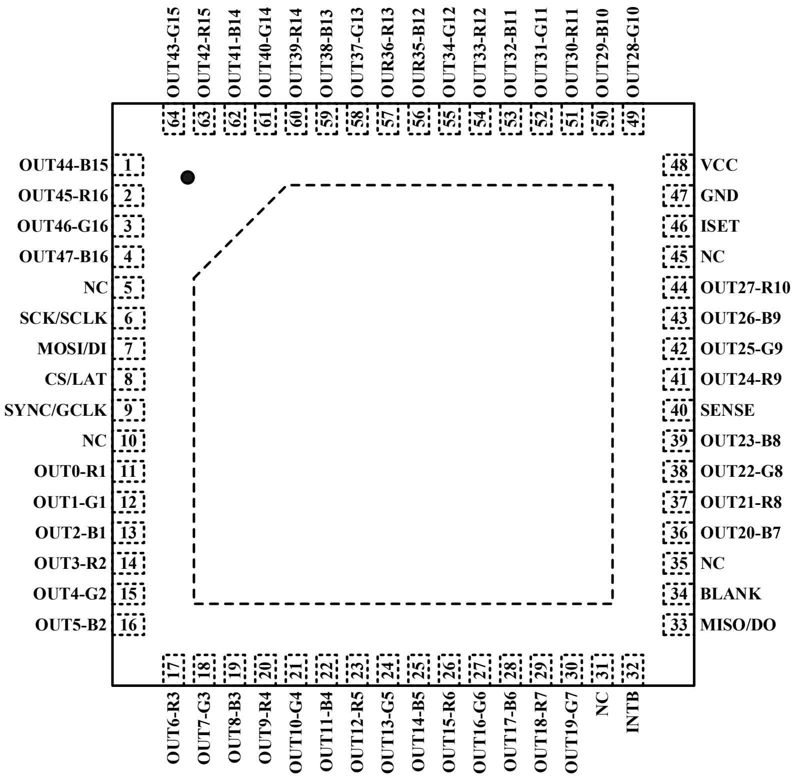
Figure 2 Typical Application Circuit (Cascade)

Note 1: The SENSE pin is short detect reference voltage, should connect to V_{LED+}.

Note 2: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS32FL3248, it is determined by V_{LED+}, I_{OUT}, V_F of LED, V_{HR} of OUTx. RLED= (V_{LED+}-V_F-VHR_{OUT})/I_{OUT}. It is optional or 39Ω recommended for white/blue/green LEDs, 68Ω recommended for red/yellow/orange LEDs when V_{LED+}=5V and single LED application.

Note 3: At least add one 10μF capacitor to V_{LED+}, if possible, it is recommended to add a 10μF to each group (R/G/B group), and this capacitor needs to close to the LEDs cathode and the ground net of the capacitor should be well connected to the GND plane.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eLQFP-64	
WFQFN-64	

PIN DESCRIPTION

No.	Pin	Description
1~4,11~30, 36~39,41~44, 49~64	OUT [0:47]	Output channel for LEDs.
5,10,31,35,45	NC	Not connect.
6	SCK / SCLK	SPI clock / VSB clock.
7	MOSI / DI	SPI input data / VSB input data.
8	CS / LAT	CS signal of SPI / Latch signal of VSB.
9	SYNC/GCLK	Synchronization.
32	INTB	Interrupt output pin. Send DEh command can read the interrupt event happens and the INTB pin active low when the interrupt event happens. Can be NC (float) if interrupt function is not used.
33	MISO / DO	SPI output data / VSB output data.
34	BLANK	Blank all outputs. BLANK low forces all channels off. PWM timing controller is initialized. BLANK high starts PWM timing controller, channels are controlled by PWM timing controller.
40	SENSE	Short detect reference voltage. The SENSE pin should connect to V_{LED+}.
46	ISET	Set the maximum I_{OUT} current.
47	GND	Ground.
48	VCC	Power supply.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32FL3248-LQLA3-TR	eLQFP-64, Lead-free	1500
IS32FL3248-QWLA3-TR	WFQFN-64, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Voltage at OUTx and SENSE pin	-0.3V ~ +18V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	21.6°C/W (WFQFN-64) 23.73°C/W (eLQFP-64)
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	5.79°C/W (WFQFN-64) 9.97°C/W (eLQFP-64)
ESD (HBM) ESD (CDM)	±4kV ±750V

Note 4: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

“♦” This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
“◊” This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
The following specifications apply for V_{CC}= 5V, T_J= 25°C, unless otherwise noted (Note 5).

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage			3		5.5	V
I_{CC}	Quiescent power supply current	R_{ISET}= 5.6kΩ, OSC= 16MHz, SL= 0xFC, GCC_X= 0xFF, CB= “111”, PWM= 0x0000, all LEDs off			12	13	mA
I_{SD}	Shutdown current	R_{ISET}= 5.6kΩ, OSC= 16MHz, SL= 0xFC, GCC_X= 0xFF, CB= “111”, PWM= 0x0000, all LEDs off, SSD=1			150	240	μA
I_{OUT}	Maximum constant current of OUTx	R_{ISET}= 5.6kΩ, V_{OUT}= 0.8V, SL= 0xFC, GCC_X= 0xFF, CB= “101”, PWM= 0xFFFF			24.8		mA
		R_{ISET}= 5.6kΩ, V_{OUT}= 0.8V, SL= 0xFC, GCC_X= 0xFF, CB= “111”, PWM= 0xFFFF			33.8		
ΔI_{MAT}	Output current error between outputs (Note 6)	R_{ISET}= 5.6kΩ, V_{OUT}= 0.8V, SL= 0xFC, GCC_X= 0xFF, CB= “101”, PWM= 0xFFFF	♦	-3		3	%
			◊	-5		5	%
ΔI_{ACC}	Output current error between devices (Note 7)	R_{ISET}= 5.6kΩ, V_{OUT}= 0.8V, SL= 0xFC, GCC_X= 0xFF, CB= “101”, PWM= 0xFFFF	♦	-3		3	%
			◊	-6		6	%
I_{OZ}	Output leakage current	SSD=1, PWM=0x0000, V_{OUT}=5.0V	♦			0.5	μA
			◊			1	μA
V_{HR}	Current sink headroom voltage OUTx	R_{ISET}= 5.6kΩ, SL= 0xFC, GCC_X= 0xFF, PWM= 0xFFFF, CB= “111”, I_{SINK}= 33mA			350	450	mV

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 5V, T_J= 25°C, unless otherwise noted (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OD}	LED open detect threshold	I_{OUT}≥ 0.1mA, PWM> 25%, measured at OUTx LODVTH= "00", Minimum level 1	0.05	0.09		V
		I_{OUT}≥ 0.1mA, PWM> 25%, measured at OUTx LODVTH= "01", Minimum level 2	0.15	0.19		
		I_{OUT}≥ 0.1mA, PWM> 25%, measured at OUTx LODVTH= "10", Minimum level 3	0.30	0.35		
		I_{OUT}≥ 0.1mA, PWM> 25%, measured at OUTx LODVTH= "11", Minimum level 4	0.44	0.49		
V_{SD}	LED short detect threshold	I_{OUT}≥0.1mA, PWM> 25%, LSDVTH= "1", measured at (V_{SENSE}-V_{OUT})		0.3		V
V_{ISET}	Voltage of ISET pin	R_{ISET}= 5.6kΩ		1.19		V
f_{OUT}	PWM frequency of output	OSC= 16MHz, PWM mode=16-bit mode		244		Hz
		OSC= 16MHz, PWM mode=8+8-bit mode PWM> 0x0100		62.5		kHz
I_{PT}	LED protect current	V_{OUT}= 0.8V, SL= 0xFC, GCC_X= 0xFF, CB= "111", PWM= 0xFFFF		75		mA
T_{SD}	Thermal shutdown	(Note 8)		165		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 8)		20		°C
Logic Electrical Characteristics (MOSI/DI, MISO/DO, CS/LAT, SCK/SCLK, BLANK)						
V_{IL}	Logic "0" input voltage	V_{CC}= 3V~5.5V	GND		0.3V_{CC}	V
V_{IH}	Logic "1" input voltage	V_{CC}= 3V~5.5V	0.7V_{CC}		V_{CC}	V
V_{OH}	H level pin output voltage	I_{OH}= -2mA	V_{CC}-0.4V		V_{CC}	V
V_{OL}	L level pin output voltage	I_{OL}= 2mA	0		0.4	V
V_{OL}	L level pin output voltage (INTB)	I_{OH}= 1mA	0		0.4	V
I_{IL}	Logic "0" input current	V_{INPUT}= L (Note 8)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= H (Note 8)		5		nA

DIGITAL INPUT SPI PSWITCHING CHARACTERISTICS (NOTE 8)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		25	MHz
t_{CH}	Clock high pulse duration	10			ns
t_{CL}	Clock low pulse duration	10			ns
t_{SICH}	MOSI to Clock rising edge setup time	5			ns
t_{CLCH}	CS falling edge to Clock rising edge	33			ns
t_{CHSI}	Clock rising edge to MOSI hold time	3			ns
t_{CLCH}	Clock falling edge to CS rising edge hold time	10			ns
t_{CSH}	CS high pulse duration	60			ns
t_{SOR}	MISO rise time		25		ns
t_{SOF}	MISO fall time		25		ns
t_{CHSO}	Clock rising edge to MISO		30		ns

DIGITAL INPUT VSB PSWITCHING CHARACTERISTICS (NOTE 8)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		25	MHz
t_{CH}	Clock high pulse duration	10			ns
t_{CL}	Clock low pulse duration	10			ns
t_{DICH}	DI to Clock rising edge setup time	5			ns
t_{LLCH}	LAT falling edge to Clock rising edge	33			ns
t_{CHDI}	Clock rising edge to DI hold time	3			ns
t_{CLLH}	Clock falling edge to LAT rising edge hold time	10			ns
t_{LH}	LAT high pulse duration	60			ns
t_{DOR}	DO rise time		25		ns
t_{DOF}	DO fall time		25		ns
t_{CHDO}	Clock rising edge to DO		30		ns

Note 5: Limits are 100% production tested at 25°C. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

Note 6: I_{OUT} mismatch (channel to channel) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT}=\pm\left(\frac{I_{OUT(MAX)}-I_{OUT(MIN)}}{\left(\frac{I_{OUT0}+I_{OUT1}+...+I_{OUT47}}{48}\times 2\right)}\right)\times 100\%$$

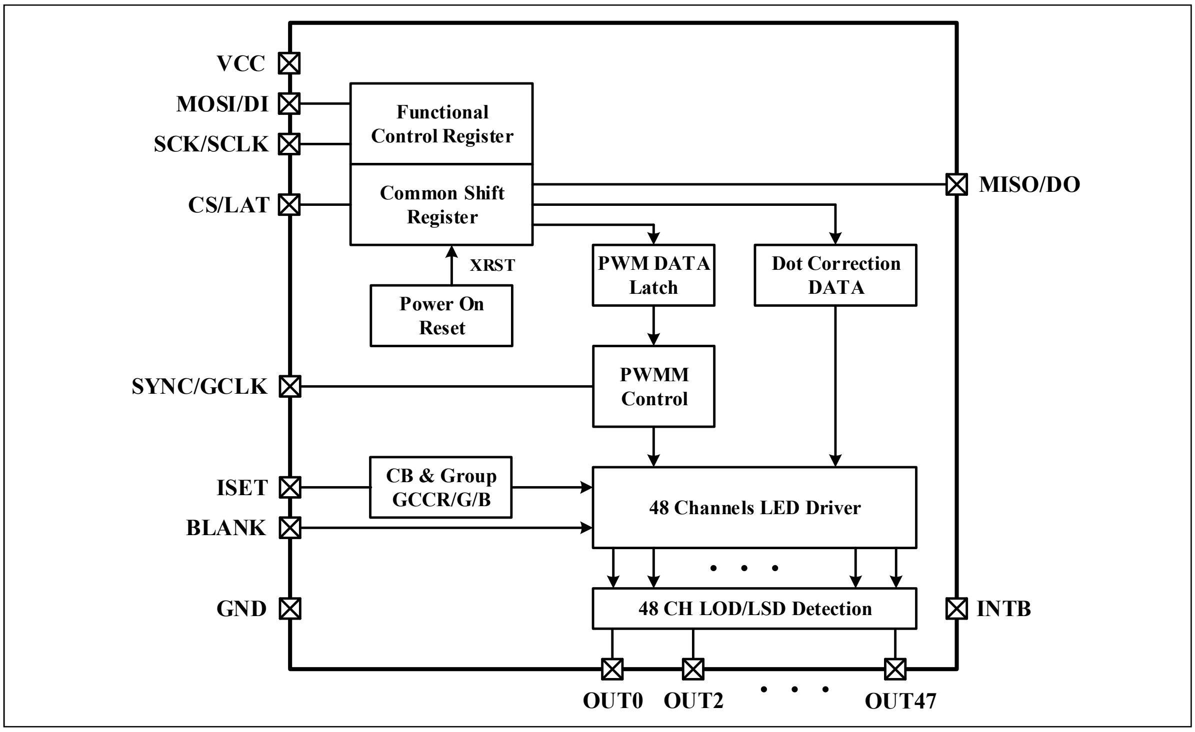
Note 7: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC}=\left(\frac{I_{OUT(MIN)}-I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right)\times 100\% \sim \left(\frac{I_{OUT(MAX)}-I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right)\times 100\%$$

Where $I_{OUT(IDEAL)}$= 24.8mA when R_{ISET}= 5.6kΩ and CB= “101”.

Note 8: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

SPI INTERFACE

IS32FL3248 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS32FL3248 latches data when CS is asserted (low to high).

The maximum SCK frequency supported in IS32FL3248 is 25MHz.

WRITING OPERATION

SPI write data format is 8-bit (byte) command followed by the register data. The command byte determines the length and function of the register data. When writing Reset/Interrupt Flag Clear Register to IS32FL3248, only the command is sent (without data). The IS32FL3248 SPI write register timing is as shown in Figure 4~7.

READING OPERATION

FC0, FC1, Interrupt flag status, open detect result and short detect result registers can be read by SPI.

To read the registers, the first command byte selects the corresponding register, followed by a CS pulse to latch after read command byte is written to IS32FL3248. Read register timing is as shown in Figure 8.

All register writes and reads command as shown in Table 1.

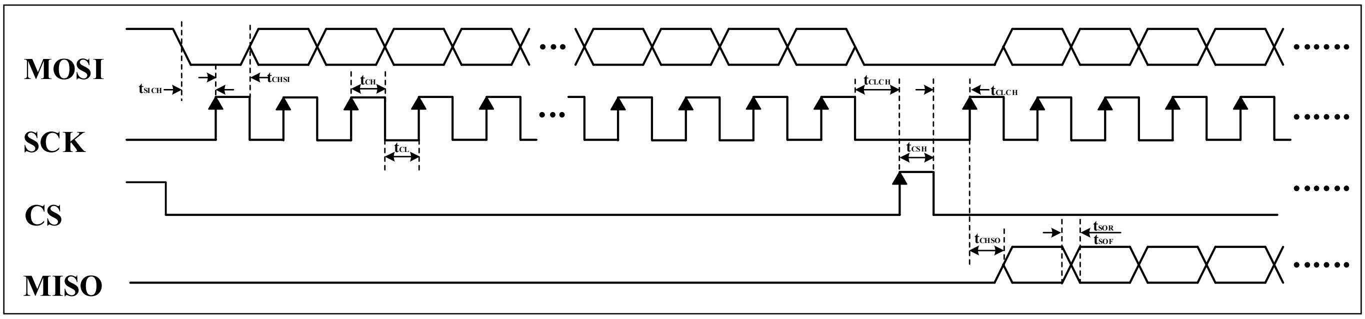


Figure 3 SPI Input Timing

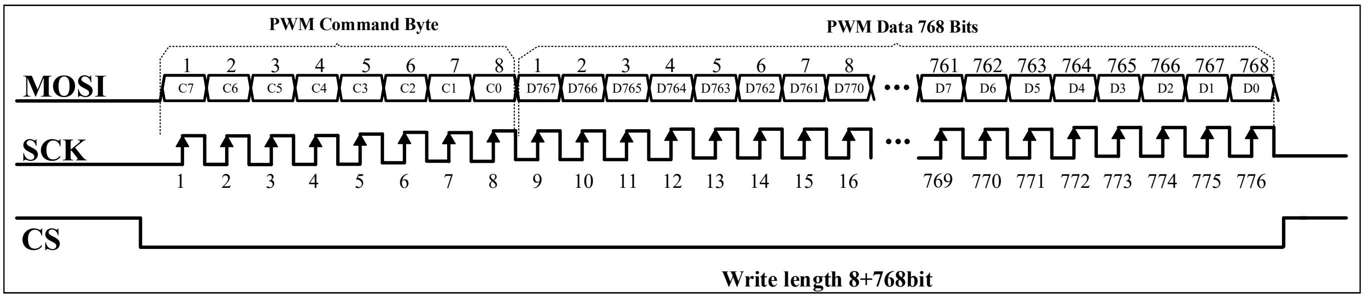


Figure 4 SPI Writing PWM Register Data to IS32FL3248

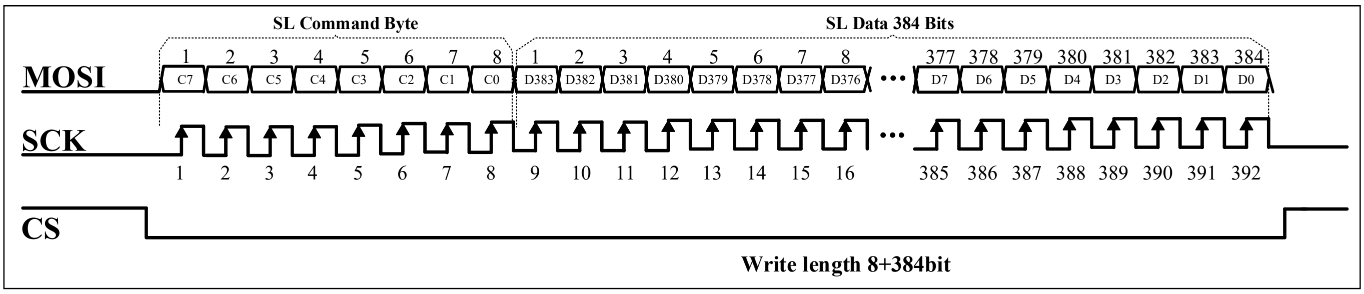


Figure 5 SPI Writing SL Register Data to IS32FL3248

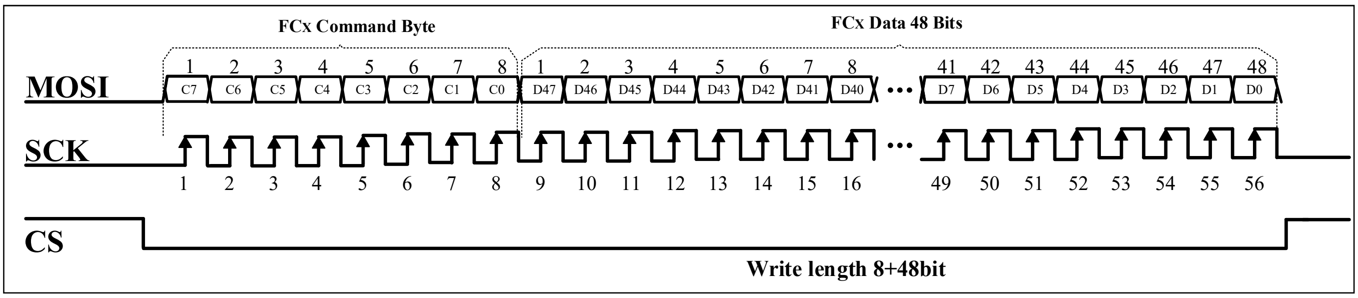


Figure 6 SPI Writing FCx Register Data to IS32FL3248

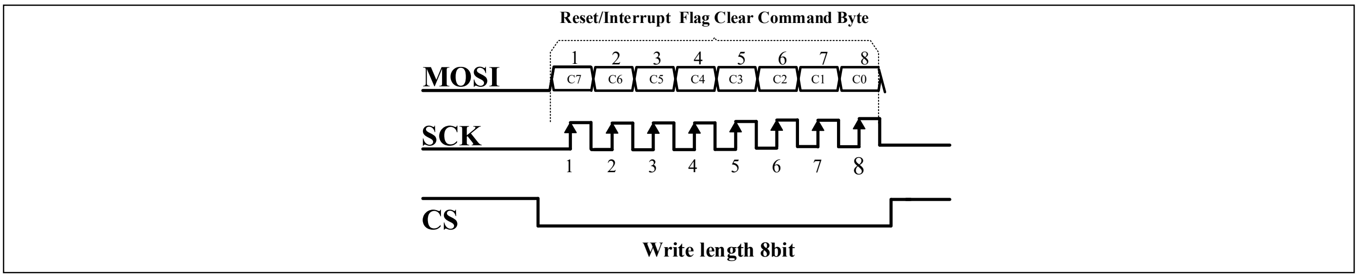


Figure 7 SPI Writing Reset/Interrupt Flag Clear Register Data to IS32FL3248

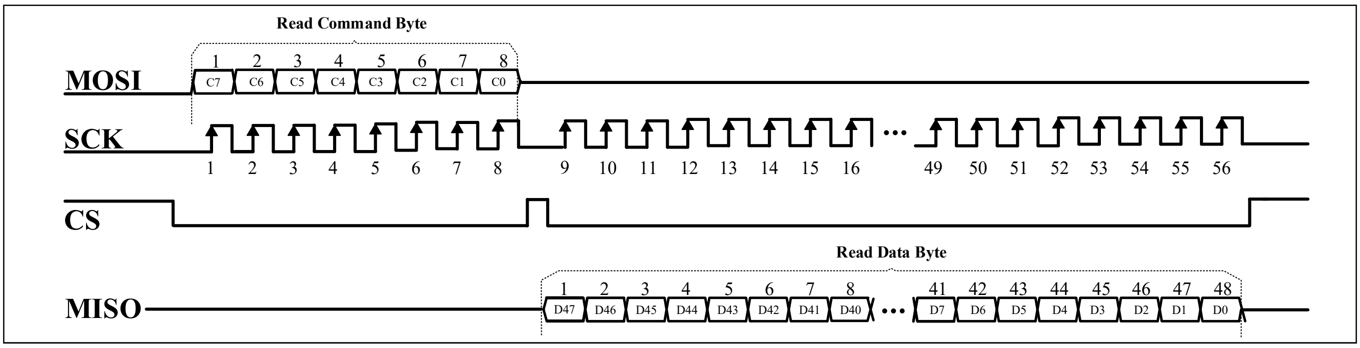


Figure 8 SPI Reading from IS32FL3248

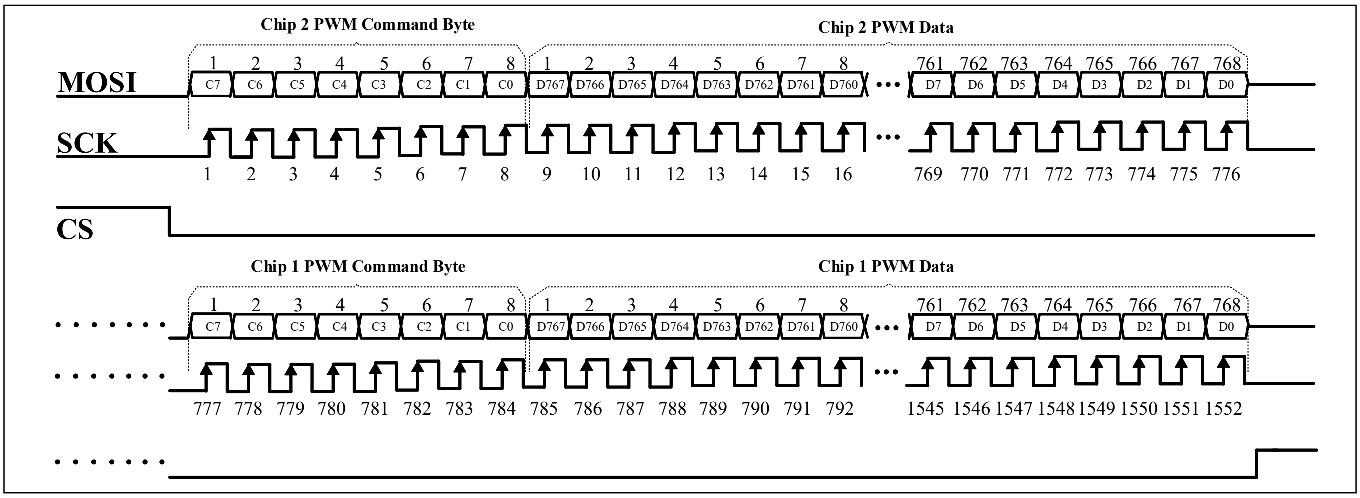


Figure 9 SPI Writing PWM Register Data to IS32FL3248 (Two Chips Cascade)

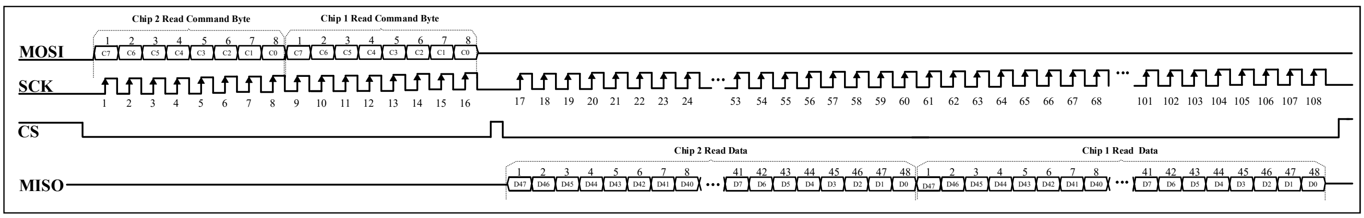


Figure 10 SPI Reading from IS32FL3248 (Two Chips Cascade)

VSB INTERFACE

IS32FL3248 uses a VSB protocol to control the chip's function with four wires: DI, SCLK, LAT and DO. VSB transfer starts from DI and SCLK controlled by Master (Microcontroller), and IS32FL3248 latches data when LAT is asserted (low to high).

The maximum SCLK frequency supported in IS32FL3248 is 25MHz.

WRITING OPERATION

VSB write data format is 8-bit (byte) command followed by the register data. The command byte determines the length and function of the register data. When writing Reset/Interrupt Flag Clear Register to IS32FL3248, only the command is sent (without data). The IS32FL3248 VSB write register timing is as shown in Figure 12~15.

READING OPERATION

FC0, FC1, Interrupt flag status, open detect result and short detect result registers can be read by VSB.

To read the registers, the first command byte selects the corresponding register, followed by a LAT pulse to latch after read command byte is written to IS32FL3248. Read register timing is as shown in Figure 16 and 17.

All register writes and reads command as shown in Table 1.

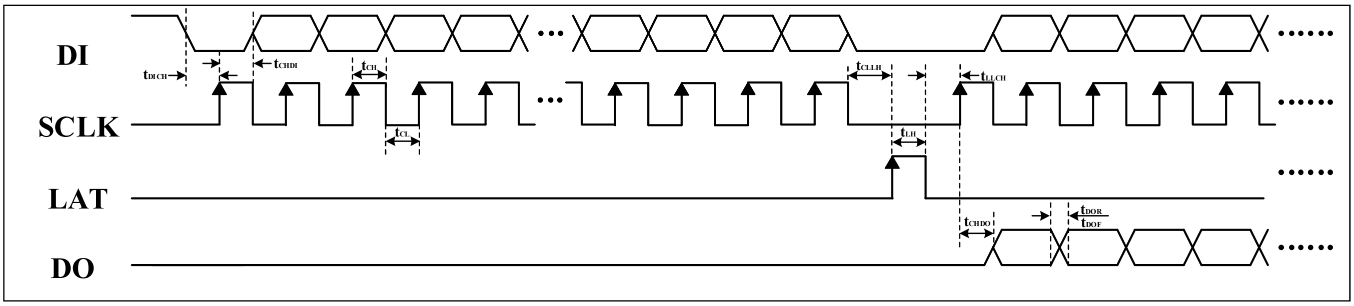


Figure 11 IS32FL3248 VSB Input Timing

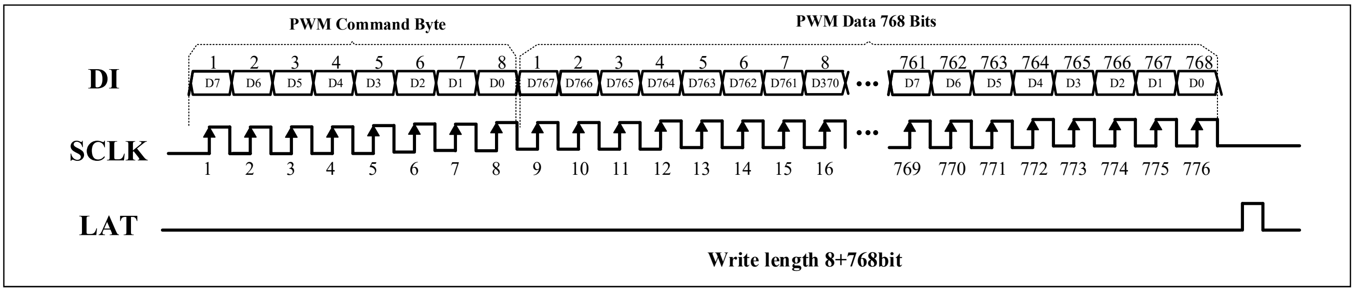


Figure 12 VSB Writing PWM Register Data to IS32FL3248

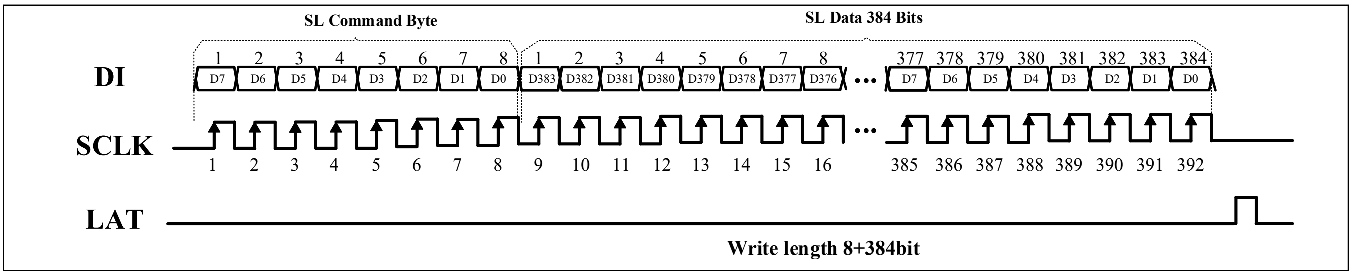


Figure 13 VSB Writing SL Register Data to IS32FL3248

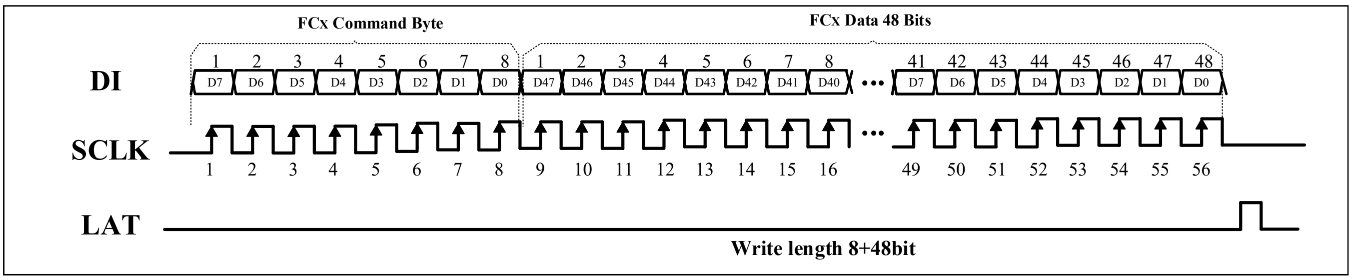


Figure 14 VSB Writing FC0/FC1 Register Data to IS32FL3248

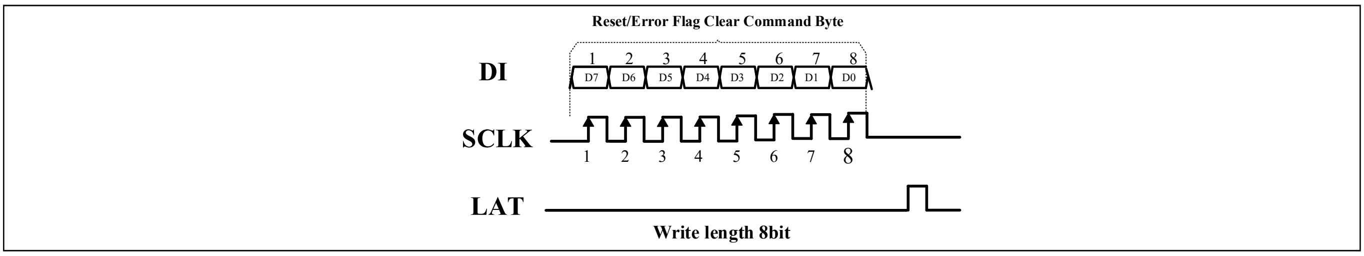


Figure 15 VSB Writing Reset/Interrupt Flag Clear Register Data to IS32FL3248

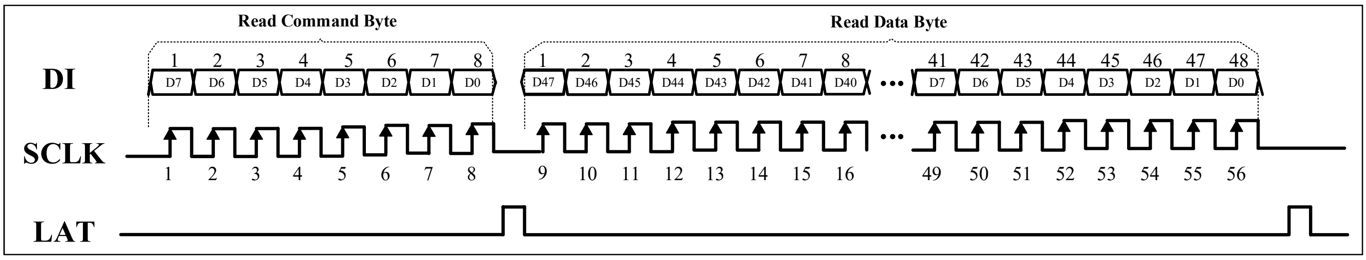


Figure 16 VSB Reading from IS32FL3248 (Bi-Direction, Read Data From DI)

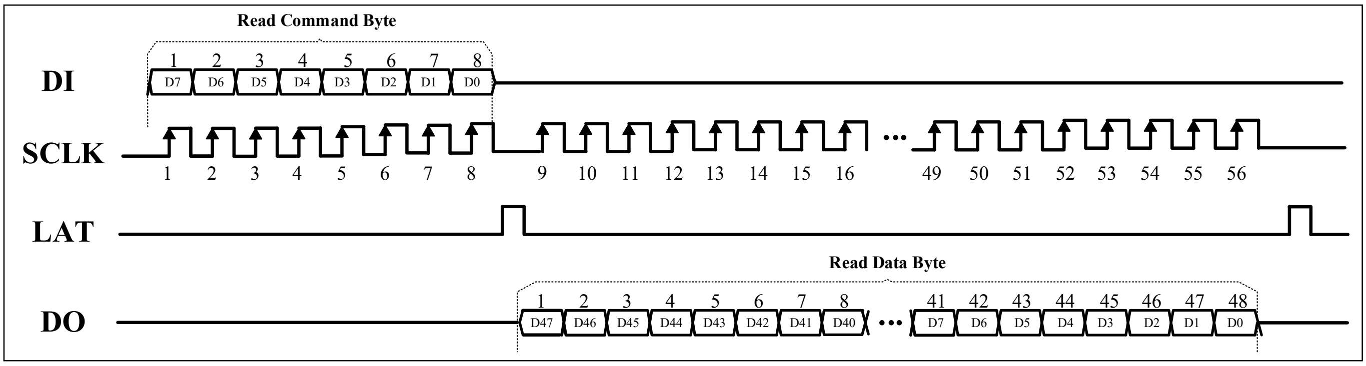


Figure 17 VSB Reading from IS32FL3248 (Single-Direction, Read Data From DO)

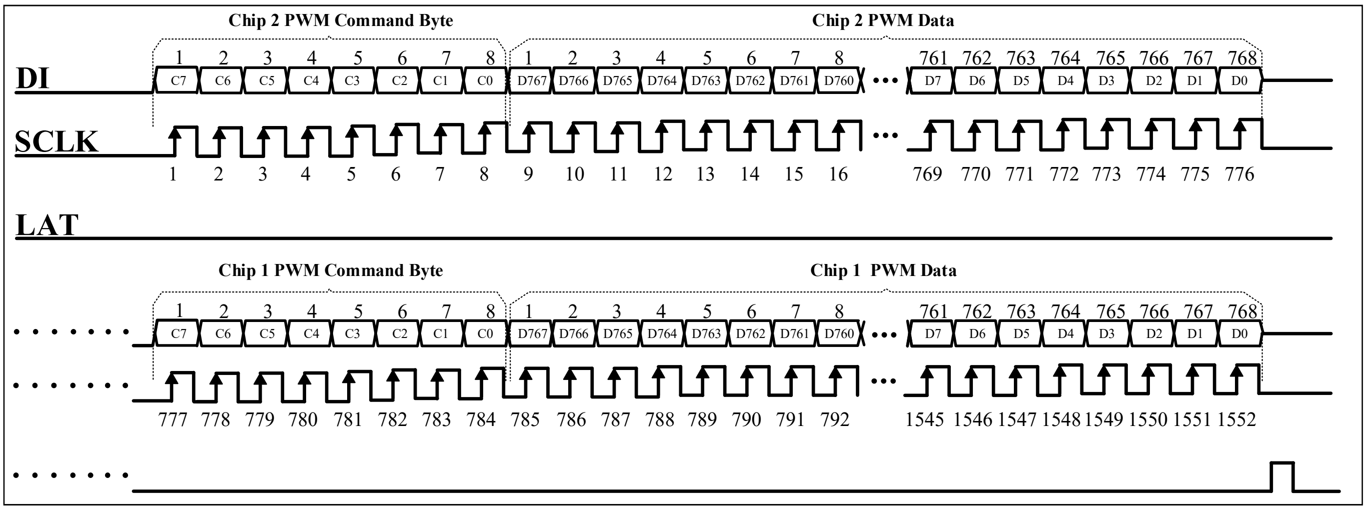


Figure 18 VSB Writing PWM Register Data to IS32FL3248 (Two Chips Cascade)

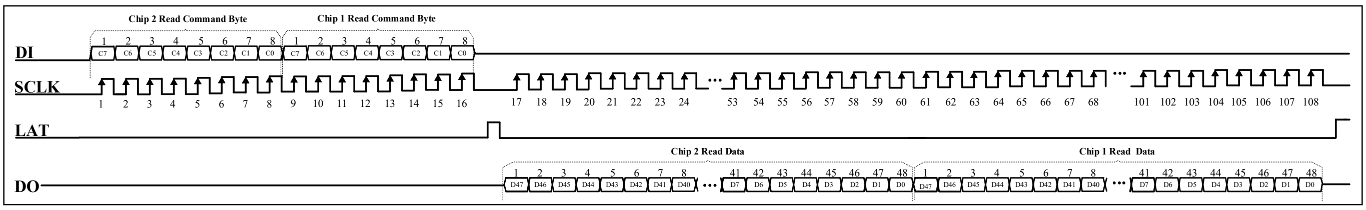


Figure 19 VSB Reading from IS32FL3248 (Two Chips Cascade)

Table 1 Register Write and Read Command

Command	Data Length	Function
0110000x	8 bits+768 bits	Write PWM Register data
0100000x	8 bits+384 bits	Write SL Register data
0010000x	8 bits+48 bits	Write FC0 Register data
1010000x	8 bits+48 bits	Read FC0 Register data
0010001x	8 bits+48 bits	Write FC1 Register data
1010001x	8 bits+48 bits	Read FC1 Register data
1011000x	8 bits+48 bits	Read open detect result of 48 channels
1100000x	8 bits+48 bits	Read short detect result of 48 channels
1101111x	8 bits+48 bits	Read interrupt flag status
0000001x	8 bits	Interrupt flag clear
0000111x	8 bits	Global reset

REGISTER DEFINITION

Table 2 Register Definition

Unit	Name	Function	Table	R/W	Default
PWM0~PWM47	PWM Register	Set PWM for each channel	3	W	0000 0000 0000 0000
SL0~SL47	SL Register	Set SL for each channel	4	W	1111 11xx
FC0	Global Current Control Register	Set global current for R channels (OUT0, OUT3 … OUT45)	5	R/W	1111 1111
		Set global current for G channels (OUT1, OUT4 … OUT46)	6	R/W	1111 1111
		Set global current for B channels (OUT2, OUT5 … OUT47)	7	R/W	1111 1111
	Current Band Register	Maximum current band control	8	R/W	011
	Configuration Register	Configure operating mode	9	R/W	01 1101
FC1	Open/Short Detect and Threshold Register and Read Direction Select Register & SYNC	Set Open/Short function and read direction & SYNC	10	R/W	1011 1010
	Frequency Selection Register and De-ghost & Spread Spectrum Register	Set OSC frequency and de-ghost & Spread Spectrum	11	R/W	0000 0000
	Phase/OUT Delay and Report Enable Register	Set phase/out delay and flag report enable	13	R/W	11 0000
	Edge Select Register	Set MOSI/DI, MISO/DO edge and MOSI/DO output delay time	14	R/W	1
	Open Action Enable Register	Set the IOUT open protection action	15	R/W	0
OP47~OP0	Open Detect Result Register	Store the open information of LED	16	R	-
ST47~ST0	Short Detect Result Register	Store the short information of LED	17	R	-
Interrupt Flag Status Read	Interrupt Flag Status Read Register	Store interrupt flag status	18	R	-
Interrupt Flag Clear	Interrupt Flag Clear Register	Interrupt flag clear	19	W	-
Reset	Reset Register	Reset all registers	20	W	-

Table 3 PWM0~PWM47 PWM Register

Unit	PWM47		…	PWM0	
Bit	767:760	759:752	…	15:8	7:0
Name	PWM_H	PWM_L	…	PWM_H	PWM_L
Default	0000 0000	0000 0000	…	0000 0000	0000 0000

PWM0~PWM47 is PWM register for OUTx. Each PWMx contains 16-bit data, control the PWM duty of each dot. Each dot has two bytes to modulate the PWM duty in 256/4096/65536 steps. If using 8-bit PWM mode, only PWM_H 8 bits need to be set.

If using 8+4-bit PWM mode, only PWM_H 8 bits and high 4 bits of PWM_L need to be set.

The channel output current, I_{OUT} and the value of the PWM registers decide the average current of each LED noted as I_{LED}.

I_{OUT} is computed by Formula (1):

$$I_{OUT} = I_{CB} \times I_{SL} \times I_{GCC} \qquad (1)$$

Where I_{CB} is current resulting from current band setting (See Table 8 Current Band Register and definitions), I_{SL} is current resulting from SL setting (See Table 4 SL Register and definitions), and I_{GCC} is current resulting from GCCx setting (See Table 5~7 GCCR/GCCB/GCCR Register and definitions).

I_{LED} computed by Formula (2):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT} \qquad (2)$$

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$ (8-bit mode)

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$ (8+4-bit mode)

N=65536: $PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$ (8+8-bit/16-bit mode)

Table 4 SL0~SL47 SL Register

Unit	SL47	…	SL0
Bit	383:376	…	7:0
Name	SL	…	SL
Default	1111 11xx	…	1111 11xx

SL0~SL47 is the SL Register for OUTx. Each SLx contains 6-bit data that controls the DC output current for each dot. Each dot has a byte (only high 6 bits need to be set) to modulate DC current in 64 steps.

The SL Register value determines the output current of each channel, noted I_{OUT}.

I_{OUT} computed by Formula (1):

$$I_{OUT} = I_{CB} \times I_{SL} \times I_{GCC} \qquad (1)$$

$$I_{SL} = 0.259 + \frac{SL}{64} \times 0.741 \qquad (3)$$

$$SL = \sum_{n=2}^{7} D[n] \cdot 2^n \qquad (4)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, I_{CB} is current resulting from current band setting (See Table 8 Current Band Register and definitions), and I_{GCC} is current resulting from GCCx setting (See Table 5~7 GCCR/GCCB/GCCR Register and definitions).

Table 5 FC0 Unit (7:0) Global Current Control Register

Bit	7:0
Name	GCCR
Default	1111 1111

Set global current for R group channels (OUT0, OUT3…OUT45)

Table 6 FC0 Unit (15:8) Global Current Control Register

Bit	15:8
Name	GCCG
Default	1111 1111

Set global current for G group channels (OUT1, OUT4…OUT46)

Table 7 FC0 Unit (23:16) Global Current Control Register

Bit	23:16
Name	GCCB
Default	1111 1111

Set global current for B group channels (OUT2, OUT5…OUT47)

The Global Current Control Register modulates all OUTx (x=0~47) global current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (1):

$$I_{OUT} = I_{CB} \times I_{SL} \times I_{GCC} \qquad (1)$$

$$I_{GCC} = 0.096 + \frac{GCC}{256} \times 0.904 \qquad (5)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (6)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 8 FC0 Unit (26:24) Current Band Register

Bit	26:24
Name	CB
Default	011

The Current Band Register stores the current band or the maximum output current range of each LED output.

$I_{OUT(MAX)}$ is the maximum current output decided by R_{ISET} (Check R_{ISET} section for more information). Example: when R_{ISET}=5.6kΩ, $I_{OUT(MAX)}$ =33mA.

I_{CB} is the maximum current band decided by CB registers.

CB Current Band Setting
000 Band 1: I_{CB}= $I_{OUT(MAX)}$ × 9.7%
001 Band 2: I_{CB}= $I_{OUT(MAX)}$ × 22.5%
010 Band 3: I_{CB}= $I_{OUT(MAX)}$ × 35.3%
011 Band 4: I_{CB}= $I_{OUT(MAX)}$ × 48.1%
100 Band 5: I_{CB}= $I_{OUT(MAX)}$ × 61.0%
101 Band 6: I_{CB}= $I_{OUT(MAX)}$ × 73.4%
110 Band 7: I_{CB}= $I_{OUT(MAX)}$ × 87.8%
111 Band 8: I_{CB}= $I_{OUT(MAX)}$ × 100%

Table 9 FC0 Unit (32:27) Configuration Register

Bit	32	31:30	29	28	27
Name	SSD	PWMM	AUTO_ UPD	DTM RST	-
Default	0	00	0	0	1

The Configuration Register sets operating mode of IS32FL3248.

When SSD is "1", IS32FL3248 enters software shutdown mode. When SSD is "0", IS32FL3248 is in normal operation.

The PWMM bits selects PWM mode, default PWM mode is 16-bit mode.

The AUTO_UPD set auto data update function of IS32FL3248. When this bit is 0, the outputs PWM duty update immediately at the next LAT rising edge for a new PWM value data write. When this bit is 1, the output PWM duty will update at the 65,536th PWM clock after the LAT rising edge for a new PWM value write. The write control of SL data is the same.

The DTMRST set display timing reset function of IS32FL3248. When this bit is 0, the output PWM duty is not reset, the outputs are not forced off and new PWM duty update immediately at LAT rising edge for a new PWM value data write. When this bit is 1, the PWM duty is reset to 0 and all outputs are forced off at the LAT rising edge for a new PWM value data write, and all output new PWM duty will update after all outputs are forced off.

SSD Software Shutdown control
0 Normal operation
1 Software shutdown

PWMM PWM Mode Select
00 16-bit
01 8+8-bit dithering
10 8+4-bit dithering
11 8-bit

ATUO_OPD Auto Data Update Mode
0 Disable
1 Enable

DTMRST Display Timing Reset Mode
0 Disable
1 Enable

Table 10 FC1 Unit (7:0) Open/Short Detect and Threshold Register and Read Direction Select Register & SYNC

Bit	7	6	5	4	3	2:1	0
Name	MS	GCLK_ EN	SIOM	LSD_ EN	LOD_ EN	LOD VTH	LSD VTH
Default	1	0	1	1	1	01	0

When two or more IS32FL3248 are cascaded, the MS bit is set to "1" for the master IS32FL3248. The master IS32FL3248's SYNC/GCLK pin will generate a clock signal to all the slave devices. To be configured as a clock slave device and accept an external clock input the slave device's MS bit must be set to "0".

Set SIOM to "1" for single direction read data mode. In this mode, read register data will be from DO pin after sending the read command. Set SIOM to "0" for Bi-direction read mode where read register data will be from DI pin after sending the read command.

LOD_EN/LSD_EN enables the open or short LED channel detection with the result stored in open/short detect result registers.

Set LODVTH/LSDVTH to select open or short detect threshold voltage. The LODVTH supports 4 gears for selection, the LSDVTH (Note 8) only support 1 gear and need to be set to "1" when the short detection function is enabled (Default value is "0").

MS Enable of SYNC Function
0 Slave mode
1 Master mode

GCLK_EN GCLK Clock Signal Output
0 Inside (no output)
1 Output

SIOM Read Direction Select
0 Read data Bi-direction
1 Read data single direction

LSD_EN Short Detection Enable
0 Disable
1 Enable

LOD_EN Open Detection Enable
0 Disable
1 Enable

LODVTH Open Detect Threshold Select
00 0.09V
01 0.19V
10 0.35V
11 0.49V

LSDVTH Short Detect Threshold Select
0 Disable (Default)
1 V_{SENSE} -0.3V

Note 8: the short detect threshold is available when LSDVTH set to “1”, and the short detection is disable when LSDCVTH set to “0”. (Default value is “0”).

Table 11 FC1 Unit (15:8) Frequency Selection Register and De-ghost & Spread Spectrum

Bit	15:14	13:12	11	10	9:8
Name	CLT	RNG	SSP	DE_GHOST	OSC
Default	00	00	0	0	00

Spread Spectrum Register set the spread spectrum (SSP) and synchronization function of IS32FL3248. When SSP is “1”, the spread spectrum function will be enabled; the CLT bits will adjust the cycle time of spread spectrum function and the RNG bits will adjust spread spectrum range of the spread spectrum function. The oscillator clock frequency has to be 16MHz or 8MHz when the spread spectrum function is enabled.

The OSC bit selects the oscillator clock frequency, default is 16MHz.

CLT Spread Spectrum Cycle Time
00 1980μs
01 1200μs
10 820μs
11 660μs

RNG Spread Spectrum Range
00 ±3%
01 ±9%
10 ±16%
11 ±24%

SSP Spread Spectrum Function
0 Disable
1 Enable (OSC need select 16MHz or 8MHz)

DE_GHOST De-ghost Function
0 Disable
1 Enable, OUTx pull up to V_{CC}-0.3V

OSC Oscillator Clock Frequency Select
00 16MHz (default)
01 8MHz
10 4MHz
11 2MHz (not recommended for 16-bit PWM mode)

Table 12 PWM Frequency

PWM Frequency	16MHz	8MHz	4MHz	2MHz
16-bit	244Hz	122Hz	-	-
8+8-bit	244Hz~ 62.5kHz	122Hz~ 31.2kHz	-	-
8+4-bit	3.9kHz~ 62.5kHz	1.95kHz~ 31.2kHz	0.98kHz~ 15.6kHz	0.49kHz ~7.8kHz
8-bit	62.5kHz	31.2kHz	15.6kHz	7.8kHz

Table 13 FC1 Unit (21:16) Phase/OUT Delay and Report Enable Register

Bit	21	20	19	18	17	16
Name	SHORT _RE	OPEN _RE	TSD _RE	REST _RE	PHASE	OD _EN
Default	1	1	0	0	0	1

When SHORT_RE is “1”, the short detect result reporting is enabled.
When OPEN_RE is “1”, the open detect result reporting is enabled.
When TSD_RE is “1”, the thermal shutdown result reporting is enabled.
When REST_RE is “1”, the ISET pin short to ground result reporting is enabled.
If reporting is enabled, the INTB pin active low when the any interrupt event happens.

SHORT_RE Short Detect Result Report
0 Disable
1 Enable

OPEN_RE Open Detect Result Report
0 Disable
1 Enable

TSD_RE Thermal Shutdown Result Report
0 Disable
1 Enable

RSET_RE ISET Pin Short to Ground Result Report
0 Disable
1 Enable

PHASE Phase Delay Enable
0 Disable
1 Enable

OD_EN OUT Delay Function
0 Disable
1 Enable

Table 14 FC1 Unit (25:22) Edge Select Register

Bit	25:24	23	22
Name	TDO	DOE	DIE
Default	11	1	0

Set TDO to select MISO/DO output delay time
Set DOE to select MISO/DO transmit edge
Set DIE to select MOSI/DI sample edge

TDO MISO/DO Output Delay Time
00 0ns
10 1ns
01 2ns
11 3ns

DOE MISO/DO Transmit at SCK Edge
0 Falling edge
1 Rising edge

DIE MOSI/DI Data Sample at SCK Edge
0 Rising edge
1 Falling edge

Table 15 FC1 Unit (26) Open Action Enable Register

Bit	26
Name	OPEN_ACTION_EN
Default	0

The OPEN_ACTION_EN is set to the I_{OUT} open protection action when open happen.
If OPEN_ACTION_EN bit is set to "0", the I_{OUT} open protection is disable, the $I_{OUT}=I_{OUT(MAX)}$ when open happens.
If OPEN_ACTION_EN bit is set to "1", the I_{OUT} open protection is enable, the $I_{OUT}=I_{OUT(MAX)} \times 1/4$ when open happens.

Table 16 OP47~OP0 Unit (47:0) Open Detect Result Register (Read Only)

Bit	47:0
Name	OP47:OP0
Default	-

When LOD_EN (D3 of FC1) is set to "1", open detection will be enabled, and the LED open status will be detected in real time, the open status information will be stored in this register.
When read open detect result command (0xB0) is sent to IS32FL3248, then all channels open status information is read from this register. The read open detect result register timing is as shown in figure 9/17/18.

Table 17 ST47~ST0 Unit (47:0) Short Detect Result Register (Read Only)

Bit	47:0
Name	ST47:ST0
Default	-

When LSD_EN (D4 of FC1) is set to "1", short detection will be enabled and the LED short will be detected in real time. The short status information will be stored in this register.
When read short detect result command (0xC0) is sent to IS32FL3248 then all channels short status information is read from this register. The read short detect result register timing is as shown in figure 9/17/18.

Table 18 Interrupt Flag Read (DEh) Unit (7:0) Interrupt Flag Status Read Register (Read Only)

Bit	7:4	3	2	1	0
Name	-	SF	OF	TSD	RSF
Default	-	-	-	-	-

SF Short Flag
0 Normal
1 LED short detected

OF Open Flag
0 Normal
1 LED open detected

TSDF Thermal Shutdown Flag
0 Normal
1 thermal shutdown detected

RSF ISET Pin Short to Ground Flag
0 Normal
1 ISET pin short to GND detected

Table 19 Interrupt Flag Clear Unit (7:0) Register (Write Only)

Bit	7:0
Name	Interrupt Flag Clear
Default	-

When working in normal operation mode, sending Interrupt Flag Clear Command (0x02) to IS32FL3248 will clear Interrupt Flag Register status.

Table 20 Reset Unit (7:0) Reset Register (Write Only)

Bit	7:0
Name	Reset
Default	-

When working in normal operation mode, sending Reset Command (0x0E) to IS32FL3248 will reset all registers to default values.

APPLICATION INFORMATION

R_{ISET}

The maximum output current $I_{OUT(MAX)}$ for OUT0~OUT47 can be adjusted by the external resistor, R_{ISET}, as described in Formula (7).

$$I_{OUT(MAX)} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (7)$$

x= 159, V_{ISET}= 1.19V.

The recommended minimum value of R_{ISET} is 5.6kΩ.

When R_{ISET}= 5.6kΩ, $I_{OUT(MAX)}$= 33.79mA

When R_{ISET}= 7.5kΩ, $I_{OUT(MAX)}$= 25.23mA

R_{ISET} should be placed close to the chip and connected to the GND plane properly.

PWM CONTROL

The PWM Registers (PWM0~PWM47) can modulate the LED brightness of each of the 48 channels with 256/4096/65536 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is the fourth steps.

Writing varying new data continuously to the PWM registers modulates the brightness of the LEDs to achieve lighting patterns. e.g. breathing effect.

SPREAD SPECTRUM FUNCTION

PWM current switching of LED outputs can be particularly troublesome with regards to EMI. To optimize the EMI performance, the IS32FL3248 includes a spread spectrum function. By setting the RNG bit of Spread Spectrum Register, Spread Spectrum range can be chosen from ±5%, ±15%, ±24%, or ±34%. The spread spectrum function will lower the total emitting electromagnetic energy by spreading the energy into a wider frequency range to significantly degrade the EMI energy peaks. With spread spectrum, the EMI conformance test is easier to pass with a smaller and lower-cost filter circuit.

SOFTWARE SHUTDOWN MODE

Software shutdown mode can be used as a means of reducing power consumption. During software shutdown mode all registers retain their data.

By setting SSD bit of the Configuration Register (D32 of FC0) to “1”, the IS32FL3248 will operate in software shutdown mode. When the IS32FL3248 is in software shutdown mode, all current sources are switched off.

LAYOUT RECOMMEDATION

The IS32FL3248 reliability can be improved by good PCB layout. Please consider below factors when designing the PCB.

The first step to consider are the supply lines and GND connections; especially those traces with high current. The digital and analog blocks’ supply lines and GND should be separated to avoid noise from digital block affecting the analog block.

Add at least one 10μF capacitor to V_{LED+}, if possible additional 0.47μF or 1μF capacitor is recommended to connected to the ground at each power supply pins of the chip. These needs to be close to the chip and the ground net of the capacitor should be well connected to the GND plane.

1. The VCC/ V_{LED+} capacitors need to be close to the chip and the ground side should be well connected to the GND plane.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

3. The thermal pad should connect to ground plane. The PCB should have the thermal pad with 16 or 25 vias through the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of corresponding package.

4. VCC pin maximum current is less than 30mA when V_{CC}=5V, but the V_{LED+} net is providing total current of all outputs, its current can as much as 33mA×48=1584mA, recommend trace width for VCC pin is 0.15mm~0.254mm, recommend trace width for V_{LED+} net is 1.5mm~2.0mm

• Output pins=33mA, recommend trace width is 0.2mm~0.254mm

• All other pins<30mA, recommend trace width is 0.15mm~0.254mm

THERMAL CONSIDERATION

The over temperature of the chip may result in deterioration of the properties of the chip. IS32FL3248 has thermal pad but the chip could be very hot if power is very high. So, do consider the ground area connecting to the GND pins and the thermal pad. Other traces should keep clearance and ensure the ground area below the package is integrated. The backside ground layer should be connected to the thermal pad through 9 or 16 vias to maximized the ground plane area.

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise caused by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (8):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (8)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{21.6°C/W} \approx 4.63W \quad \text{(WFQFN-64)}$$

$$P_{D(MAX)} = \frac{125°C - 25°C}{23.73°C/W} \approx 4.21W \quad \text{(eLQFP-64)}$$

Figure 20, shows the power derating of the IS32FL3248 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

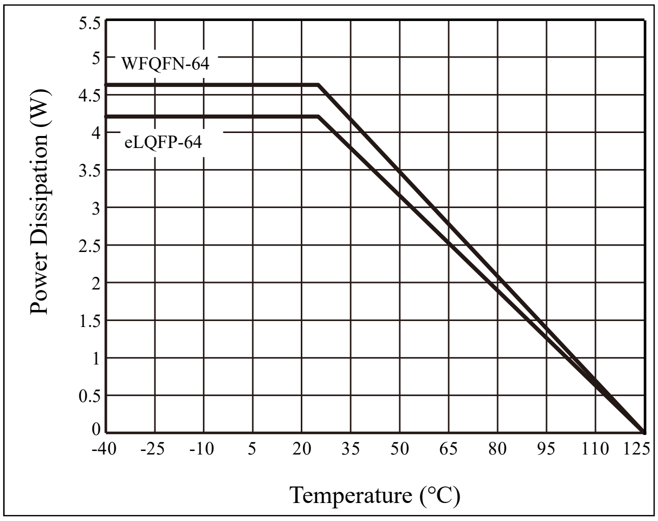


Figure 20 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

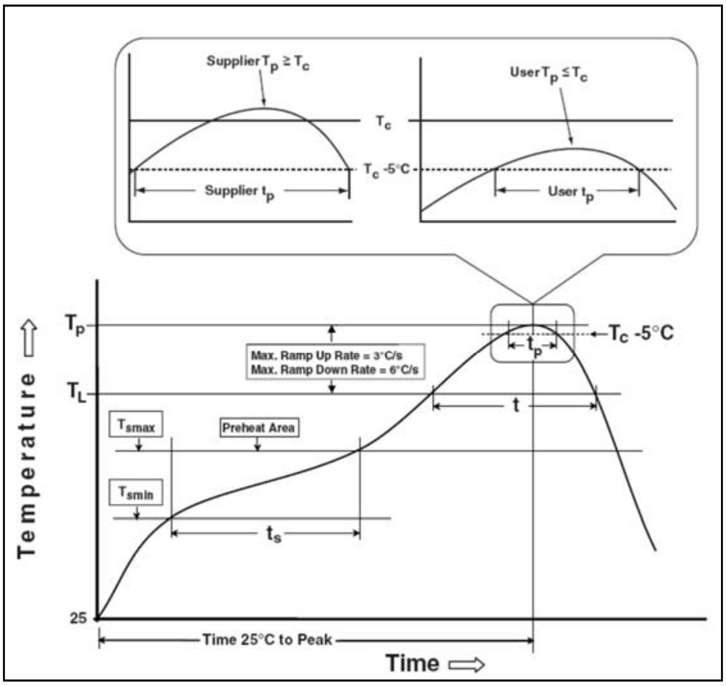
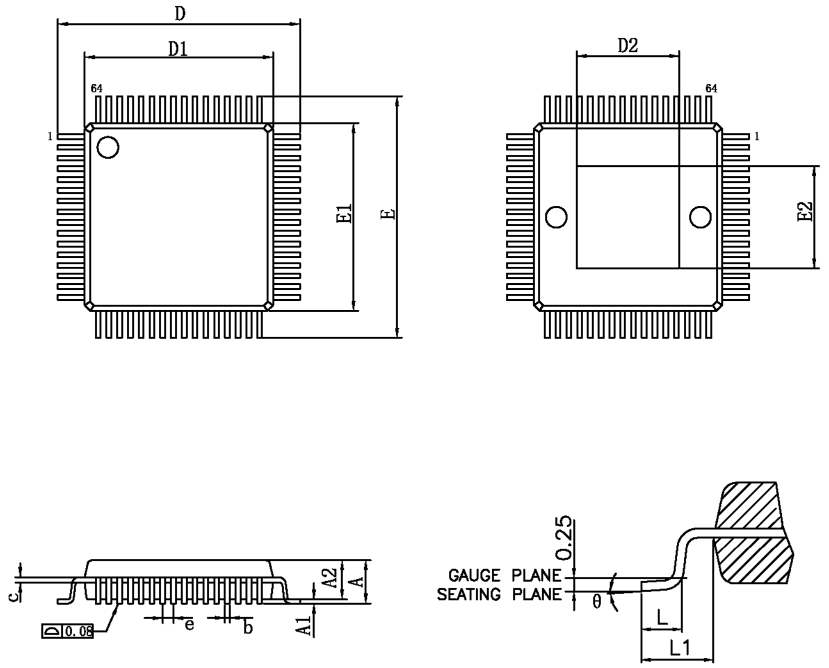


Figure 21 Classification Profile

PACKAGE INFORMATION

eLQFP-64



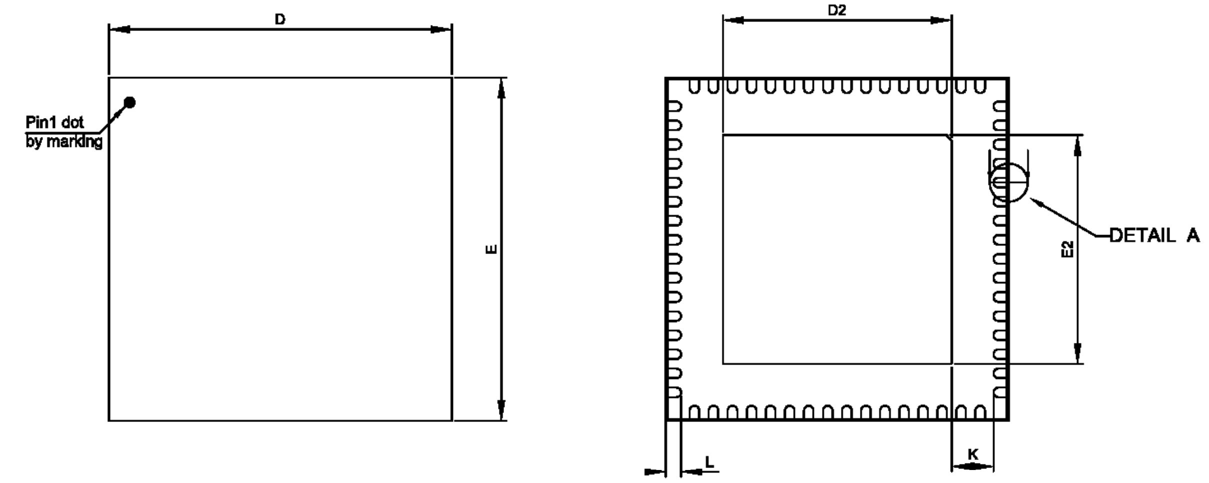
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
L1	1.0REF		
L	0.45	0.60	0.75
c	0.09	—	0.20
e	0.50BSC		
b	0.17	0.22	0.27
θ	0°	3.5°	7°
D2	3.99	4.16	4.34
E2	3.99	4.16	4.34

233-570-394 Rev. A

NOTE:

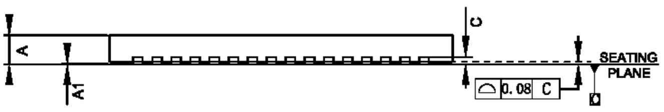
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MS-026

WFQFN-64

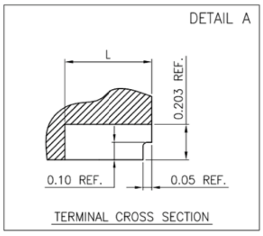


TOP VIEW

BOTTOM VIEW



SIDE VIEW



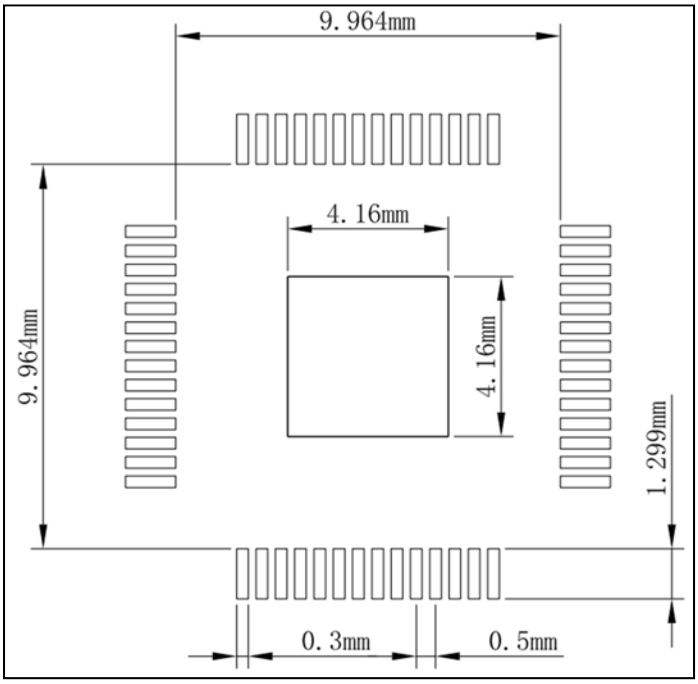
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
c	0.203 REF.		
b	0.18	0.25	0.30
D	9.00 BSC		
E	9.00 BSC		
D2	5.90	6.00	6.10
E2	5.90	6.00	6.10
L	0.35	0.40	0.45
e	0.50BSC		
K	0.20	-	-

233-570-395 Rev. A

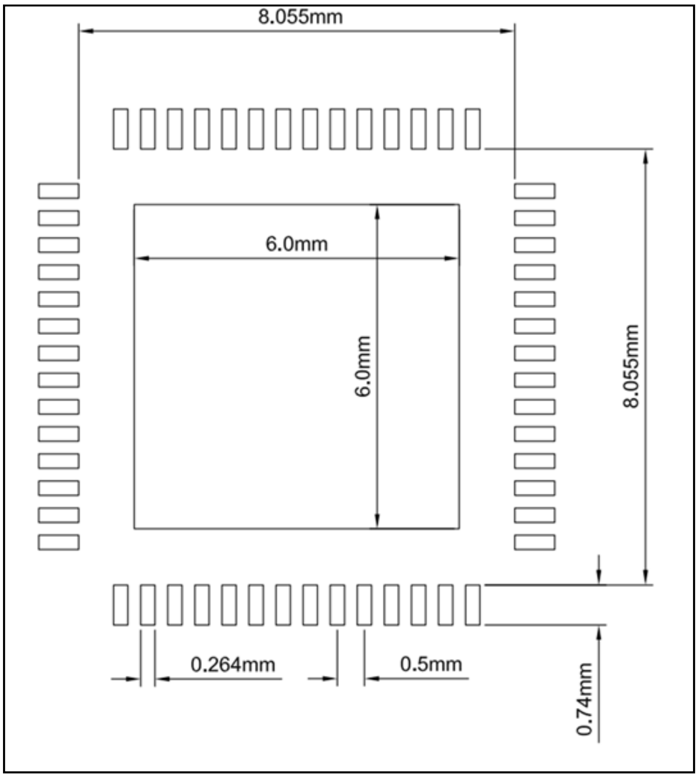
NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

eLQFP-64



WFQFN-64



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2022.07.22
0B	1.Update EC table 2.Update Read Direction Select (SIOM at Table10 (D5 of FC1)) 3.Update MISO/DO Transmit Edge (DOE at Table14 (D23 of FC1)) 4.Add PWM Frequency (Table12) 5.Add Open Action Function (OPEN_ACTION_EN at Table15 (D26 of FC1))	2023.02.01
0C	Update EC table	2023.08.21
A	Update to final version	2024.03.06