IS32FL3202

SMART LED CONTROLLER

January 2024

GENERAL DESCRIPTION

IS32FL3202 is a three channel LED controller. Each LED channel supports 6-bit DC (Dot Correction) current adjustment for color setting and 12-bit PWM for smooth LED dimming control.

The maximum output current of each LED channel (for R, G, B) is 63mA. All registers in the IS32FL3202 can be accessed via a Lumissil proprietary bus (Lumibus). IS32FL3202 supports LAA (Location Address Assignment) for random LED driver access without address pins.

IS32FL3202 can measure the LED chip temperature, which is applied to the built-in temperature compensation algorithm to provide constant luminance over wide operating temperature range. After temperature compensation, final PWM data is kept to 16-bit for more precise color presentation.

To minimize the EMI, IS32FL3202 supports spread spectrum in the PWM clock generator.

IS32FL3202 is available in WFDFN-10 (3mm×3mm), operates from 3.5V to 6.5V over the temperature range of -40°C to +125°C.

APPLICATIONS

- Automotive Ambient lighting
- Automotive Roof lighting
- Automotive Functional lighting

FEATURES

- 3.5V to 6.5V supply
- Built-in LDO to power on chip logic circuit operation
- Three 63mA R, G, B LED (1 RGB dot) drivers
- Lumissil's proprietary Lumibus supports 5V LUMI PHY and UART protocol layer for communication up to 2MHz for 128 devices or up to 1MHz for 254 devices
- LAA (Location Address Assignment) for random IS32FL3202 access without address pins, up to 254 devices can be addressed in a chain
- Broadcast mode allows all of slave devices to be addressed simultaneously
- Support 6-bit DC for each channel
- Support 12-bit PWM input data for each channel
- After temperature compensation, final PWM data is 16-bit for each channel
- Support on die OTP for binning data storage with built-in algorithm to assist fast binning production
- Support spread spectrum to reduce EMI
- Support noise reduction algorithm to minimize power ripple
- Two field PWM mode allows easier dimming and cross fading ambient light effect operation
- Provide constant luminance over wide temperature range by temperature compensation algorithm
- LED open/short detection
- Support thermal shutdown protection
- VCC under-voltage detection
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- Operating temperature: -40°C to 125°C
- WFDFN-10 (3mm×3mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

TYPICAL APPLICATION CIRCUIT

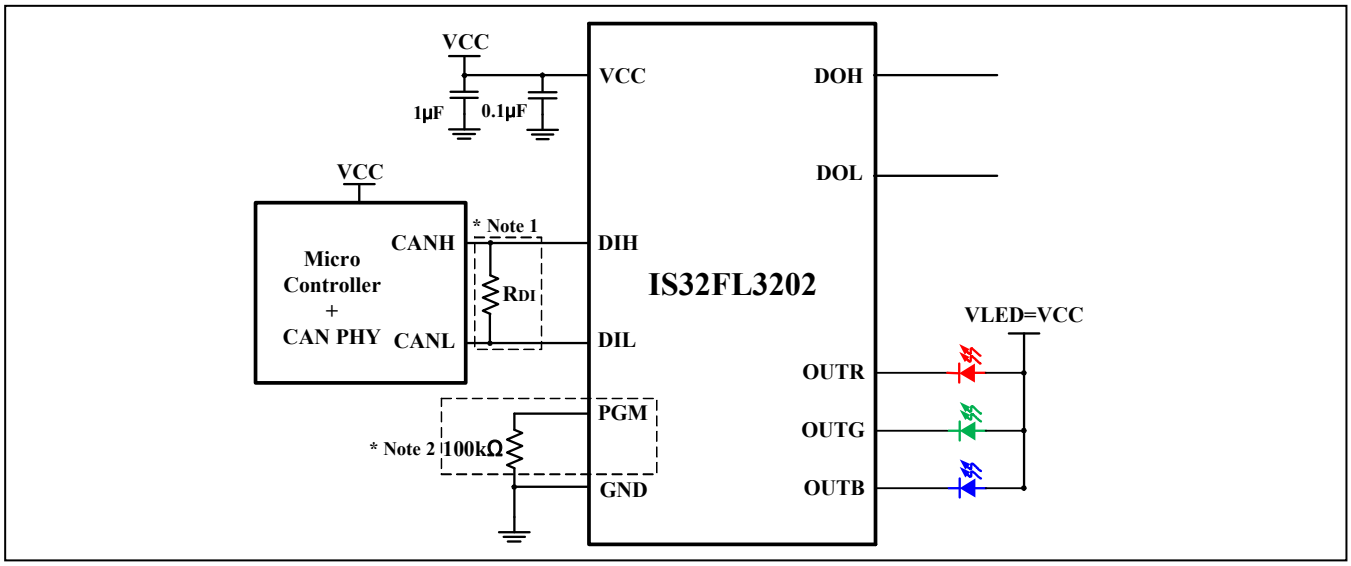


Figure 1 Typical Application Circuit

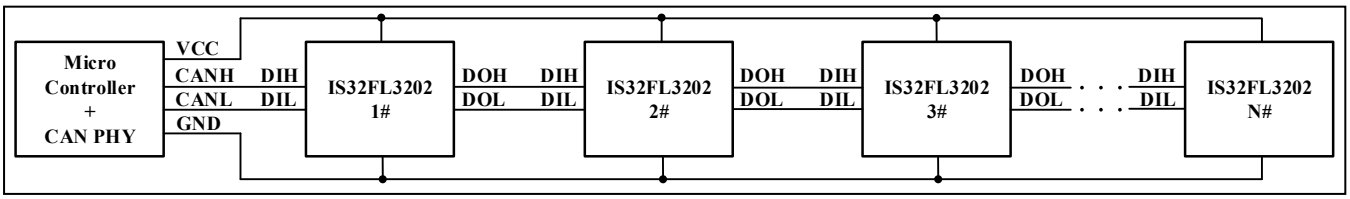
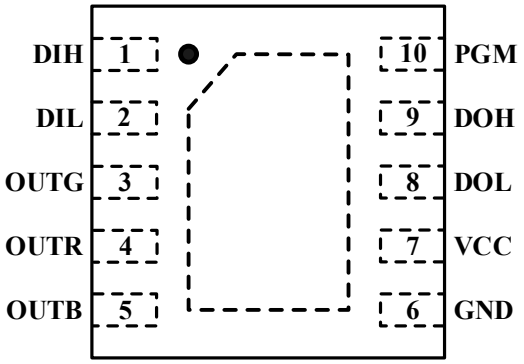


Figure 2 Typical Application Circuit (Cascade)

Note 1: It is recommended to use 120Ω for this resistor.

Note 2: During the whole on die OTP programming procedure, an external programming voltage of 4.6V~4.8V must be applied to the PGM pin and needs decoupling capacitor, and the PGM pin is recommended pull down to GND through a resistor after on die OTP programming done.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WFDFN-10	

PIN DESCRIPTION

No.	Pin	Description
1	DIH	Lumibus differential input High level.
2	DIL	Lumibus differential input Low level.
3	OUTG	Green LED driver pin.
4	OUTR	Red LED driver pin.
5	OUTB	Blue LED driver pin.
6	GND	Ground.
7	VCC	Driver power supply.
8	DOL	Lumibus differential output Low level.
9	DOH	Lumibus differential output High level.
10	PGM	On die OTP program power supply.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32FL3202-DWLA3-TR	WFDFN-10, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage VCC	-0.3V ~+8V
Voltage at any I/O pin DIH, DIL, DOH, DOL	-0.3V ~V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	53.8°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-2A), θ_{JP}	5.93°C/W
ESD (HBM) ESD (CDM)	3kV 750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
The following specifications apply for V_{CC}= 5V, T_J= 25°C, unless otherwise noted (Note 4).

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage			3.5		6.5	V
I_{CC}	Quiescent power supply current	All LEDs off, register set PSM=0			7	9	mA
I_{PSM}	Power saving mode current	All LEDs off, register set PSM=1, enter power saving mode			0.75	1	mA
$I_{OUT(MAX)}$	Maximum constant current of OUTx	V_{OUT}= 0.6V, DC=0x3F, PWM=0xFFF	♦	61	63	65	mA
			◊	59	63	67	mA
ΔI_{MAT}	Output current error between outputs (Note 5)	V_{OUT}= 0.6V, DC=0x3F, PWM=0xFFF, I_{OUT}=63mA		-3		3	%
ΔI_{ACC}	Output current error between devices (Note 6)	V_{OUT}= 0.6V, DC=0x3F, PWM=0xFFF, I_{OUT}=63mA	♦	-4		4	%
			◊	-6.5		6.5	%
V_{HR}	Current sink headroom voltage OUTx	DC=0x3F, PWM=0xFFF, I_{OUT}=63mA			350	450	mV
f_{OUT}	PWM frequency of output	Frequency setting= 244Hz		230	244	258	Hz
T_{SD}	Thermal shutdown	(Note 7)			165		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 7)			25		°C
V_{OC}	OUTx open threshold	DC= 0x1E, I_{OUT}= 30mA, PWM>1%, measured at OUTx		220	310		mV
V_{SC}	OUTx short threshold	PWM>1%, measured at (V_{CC}-V_{OUTX})		400	600		mV
I_{LEAK}	R/G/B channel leakage current	V_{OUTX}= 5V, V_{CC}= 5V				0.25	μA

LUMIBUS INTERFACE CHARACTERISTICS (NOTE 7)

The following specifications apply for T_J= 25°C, unless otherwise noted (Note 4).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{O_DOM}	Dominant output voltage	V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, measured at DOH pin	V_{CC} -0.3	V_{CC} -0.1	V_{CC}	V
		V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, measured at DOL pin	0	0.1	0.3	V
V_{DOMSYM}	Dominant voltage symmetry	V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, V_{DOMSYM}= V_{CC}-V_{DOH}-V_{DOL}	-200		+200	mV
V_{TXSYM}	Transmitter voltage symmetry	V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, V_{TXSYM} = V_{DOH}+V_{DOL}	V_{CC} -0.3		V_{CC} +0.3	V
V_{O_RES}	Recessive output voltage	V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, measured at DOH and DOL pin		0.5× V_{CC}		V
V_{O_DIF}	Differential output voltage	Dominant: V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, V_{O_DIF}=V_{DOH}-V_{DOL}	1.5		V_{CC}	V
		Recessive: V_{CC} = 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, V_{O_DIF} =V_{DOH}-V_{DOL}	-50		+50	mV
V_{REC_RX}	Receiver input differential recessive voltage	Recessive: V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, V_{REC_RX} =D_{IH}-D_{IL}, 0V≤V_{DIL}≤V_{CC}, 0V≤V_{DIH}≤V_{CC}			0.5	V
V_{DOM_RX}	Receiver input differential dominant voltage	Dominant: V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, V_{DOM_RX}= D_{IH}-D_{IL}, 0V≤V_{DIL}≤V_{CC}, 0V≤V_{DIH}≤V_{CC}	0.9			V
V_{HYS_DIF}	Differential receiver hysteresis voltage	V_{CC}= 3.5V to 6.5V, wake up modes, R_L ≥1000Ω, 0V≤V_{DIL}≤V_{CC}, 0V≤V_{DIH}≤V_{CC} (Note 7)		100		mV
I_{O_DOM}	Dominant short-circuit output current	V_{CC}= 3.5V to 6.5V, wake up modes, DOH short to ground, measured DOH pin output current		-20	-15	mA
		V_{CC}= 3.5V to 6.5V, wake up modes, DOL short to VCC, measured DOL pin output current	15	20		mA
I_{O_RES}	Recessive short-circuit output current	V_{CC}= 3.5V to 6.5V, DOH short to ground, measured DOH pin output current		-1		mA
		V_{CC}= 3.5V to 6.5V, DOL short to VCC, measured DOL pin output current		1		mA
R_{I_DIF}	Differential input resistance	measured at DIH and DIL pin		1.7		kΩ
R_{O_DIF}	Differential output resistance	measured at DOH and DOL pin		1.7		kΩ

Note 4: Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

Note 5: I_{OUT} mismatch (channel to channel) △I_{MAT} is calculated: $\Delta I_{MAT} = \pm\left(\frac{I_{OUT(MAX)}-I_{OUT(MIN)}}{\left(\frac{I_{OUT1}+I_{OUT2}+I_{OUT3}}{3}\times 2\right)}\right)\times 100\%$

Note 6: I_{OUT} accuracy (device to device) △I_{ACC} is calculated:

$$\Delta I_{ACC} = \left(\frac{I_{OUT(MIN)}-I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right)\times 100\% \sim \left(\frac{I_{OUT(MAX)}-I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right)\times 100\%$$

Where $I_{OUT(IDEAL)}$= 63mA

Note 7: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM

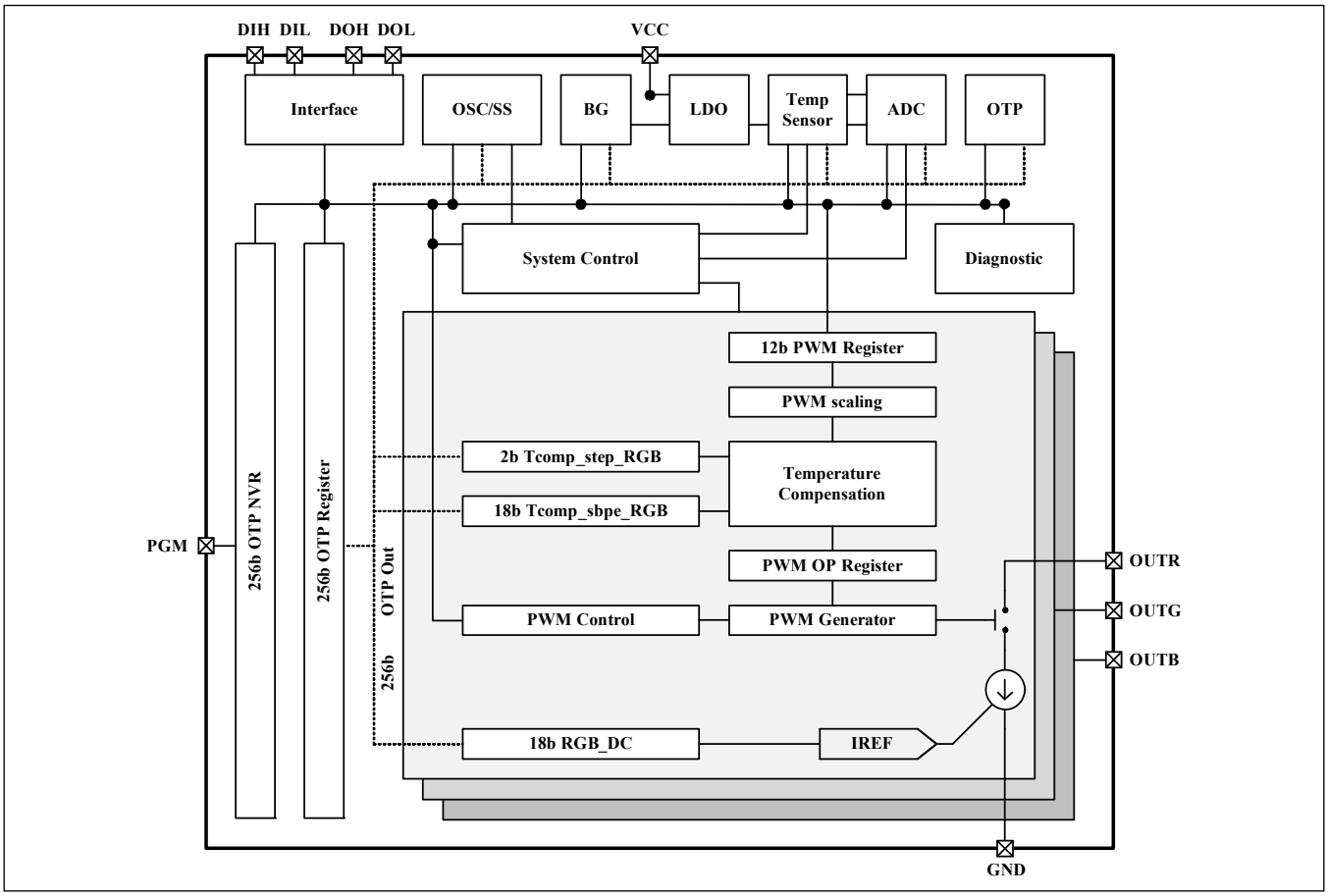


Figure 3 IS32FL3202 Block Diagram

IS32FL3202 can control R, G, and B LED individually, as shown in the above block diagram. Each LED channel can support up to 63mA current. For the best thermal performance, in addition to a good package thermal resistance and a good multiple layer PCB, an external buck controller is recommended to lower VCC to minimum LED headroom's operating voltage.

Many parameters can be adjusted via a Lumissil proprietary bus, Lumibus, for communication. Lumibus has two major components: LUMI PHY and UART protocol layers. The PHY protocol is based on the simplified, 5V CAN PHY protocol, and is only used to convert CAN PHY like transmission signaling to the ordinary UART signaling for internal processing. More CAN PHY specific features are not supported, such as sleep and wake up signaling.

Because of its differential nature, IS32FL3202's Lumibus offers a very robust and proven communication means, reducing EMI/EMC emission, and less susceptible to external RF interference.

UART protocol is used on the data link layer. In order to send proper controlling parameters to the specific registers of a specific device in the system, each device needs a unique address (Network Address, NAD) and each register needs a unique register address. A Location Address Assignment (LAA) method is used for automatic address assignment. This method allows all identical IS32FL3202 devices in the system to be assigned one unique NAD, which is stored in the on-die OTP permanently. OTP itself is protected by an ECC code for reliable NAD storage.

The on-die OTP stores many trimming and calibration parameters, such as binning and temperature compensation information. Lumissil can provide production GUI tools for ease of trimming and calibration production flow.

Additional measures are taken to further reduce EMI emission, such as audible and power ripple reduction method, as well as spread spectrum for PWM modulation, which is very important for commercial and auto applications.

DETAILED DESCRIPTION

LUMIBUS INTERFACE

Lumibus System Architecture

IS32FL3202 uses Lumissil's proprietary Lumibus for communication. Lumibus adopts the matured and proven UART protocol layer and 5V CAN PHY protocol layer. The system host communicates (write and read) with slaves via Lumibus utilizing two signal wires: DIH and DIL as shown in Figure 4. Each chain is connected to the MCU via a commercial CAN PHY.

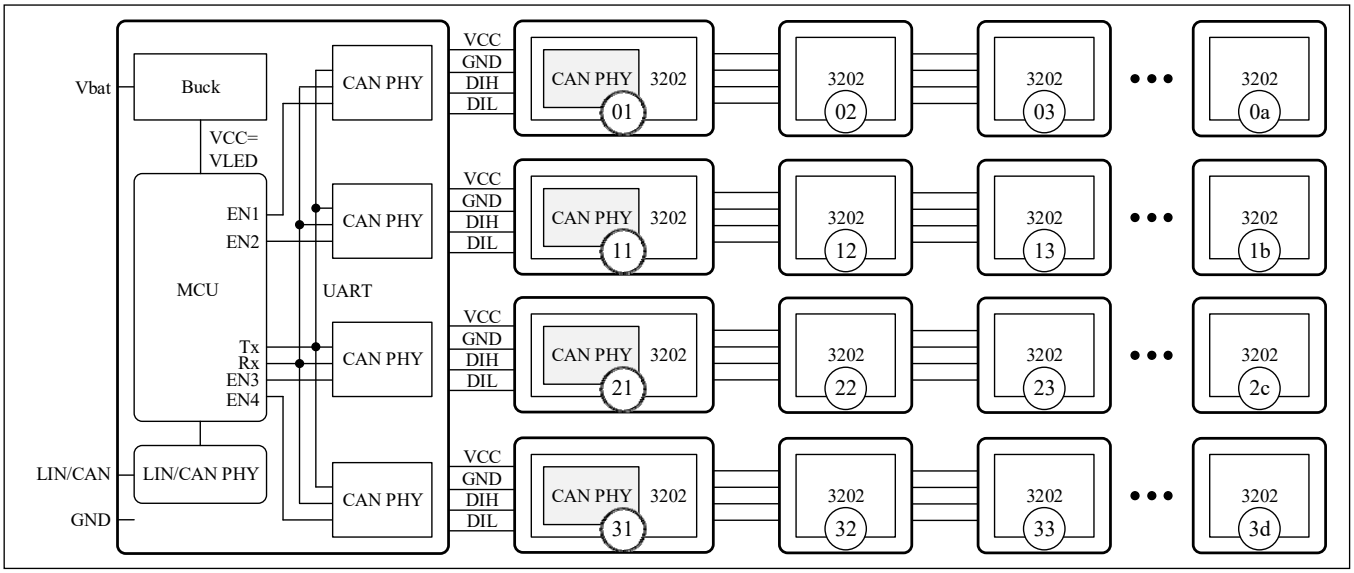


Figure 4 Lumibus System Topology (One Module In A Zone)

Prior to the system operation, Location Address Assignment (LAA) method is used to automatically assign address for each Lumibus slave device in each chain. LAA address can be stored either in the on-die OTP for permanent storage, so that LAA algorithm only needs to be executed for the first time out of factory, or in the on-die LAA register, so that LAA algorithm needs to be executed every time the system's power is applied. Detailed LAA method is described later.

The MCU issues PWM data to the addressed slave device, e.g., IS32FL3202, to control each LED's color and brightness. The PWM data that is issued by the MCU is pre-processed, including various color space conversion and optionally gamma correction.

Each device is individually calibrated to compensate for LED production variations, and the calibrated parameters can be stored in an on-die, non-volatile, one-time-programmable memory, OTP. The parameters that are stored in this OTP is retrieved during system initialization and are copied to the corresponding accessible registers for operation.

The LED driver controller inside IS32FL3202 measures temperature periodically and adjusts PWM duty cycle accordingly for each LED channel to maintain a constant luminance that is set at room temperature over wide temperature range (-40°C to 125°C). The device temperature is measured and obtained via an integrated analog-digital converter (ADC).

Besides the temperature measurement, the ADC can also measure various other analog parameters. These measurements are always triggered by a command from the host. The result of the corresponding ADC conversion can be read by a host command.

Simplified CAN PHY Format

A pair of LUMI PHY, one for receiving incoming signal and one for driving the next IS32FL3202 in the daisy chain, is integrated inside ISFL323202, using VCC as bias, which timing is shown in Figure 5. It can communicate with external, commercial CAN PHY directly if it is also biased with the same VCC for voltage compatibility.

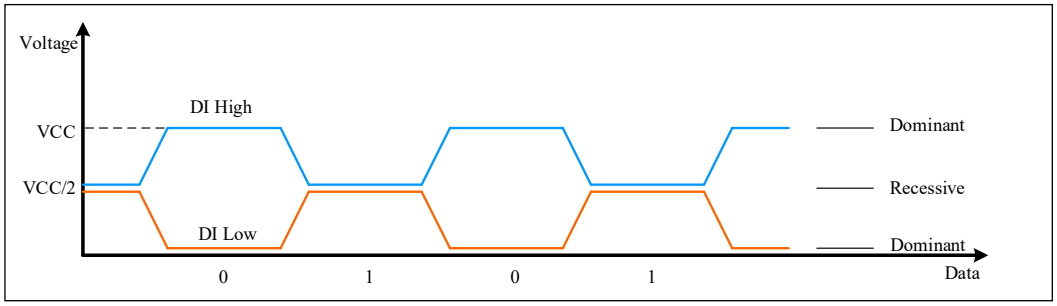


Figure 5 IO Timing On Lumibus: Adopted From CAN Bus; Maximum Voltage Swing Is ±V_{CC}/2.

System Power up and Operation

All IS32FL3202 slaves are configured as downstream mode after power up, e.g., from host to the daisy chained devices, ready for write operation. The system becomes upstream from slave to host only during read respond operation. Read operation is mainly for error status polling, but all registers can be read for diagnosis and calibration purpose. All commands to slaves are initiated by the system host, which are described in detail later. The minimum and maximum bandwidth of Lumibus is 0.1Mbps and 2Mbps.

After VCC is applied, before any write operation, each IS32FL3202 device has an internal power up sequence to carry out a number of operations, e.g., read out 256-bit content from OTP non-volatile memory to its corresponding OTP content registers for operation. Consequently, a minimal of 100μs is required for the host to initiate the first host command.

The system operation can start after all configuration is finished. In most cases, the default values in the configuration registers, in conjunction with the OTP content registers, are sufficient for proper operation without any change. The host only need to send proper PWM values to the downstream devices.

Inside IS32FL3202, periodically the temperature sensor will automatically read the temperature sensor, which is used to compensate for the LED color change. Temperature compensation only takes place at the PWM boundaries.

It is recommended for the host to poll each device's error status register periodically.

The host communicates with slaves via UART communication protocol described below.

Lumibus Format

UART Data Format

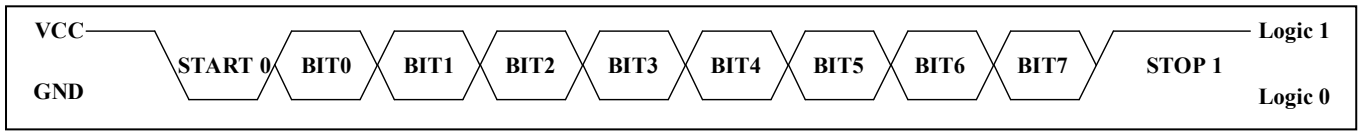


Figure 6 UART Data Byte Format

Between data frames, at least one bit is required as STOP bit, it is recommended that the host use 2-bit stop bit.

Protocol: UART Protocol (not including special command)

CMD Frame Header	Device ID	Register Start Address	N Bytes of Data	CRC checksum
1 Byte	1 Byte	1 Byte	N Bytes	2 Bytes

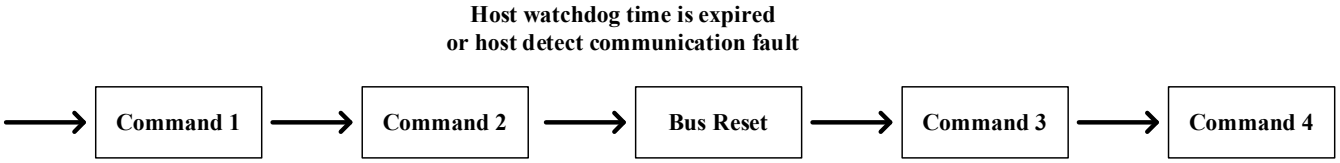
Device ID is established via Location Address Assignment (LAA) method during the first system initialization process.

Lumibus Communication Sequence

Bus Reset

When the system is powered up, normally the system host is initialized before initializing peripherals. Before initializing Lumibus devices, a bus reset operation is required.

When more than 150μs are asserted (pulled low), the host is issuing a bus reset command for bus reset operation. Upon receiving the bus reset command, all devices on the Lumibus will be in reset status. This operation can be optionally performed by the host for a number of application scenarios: (1) during system power up, as stated above, (2) host watchdog time is expired, (3) Lumibus communication fault is detected, illustrated as in the following diagram:



Bus Reset and SYNC Command Frame

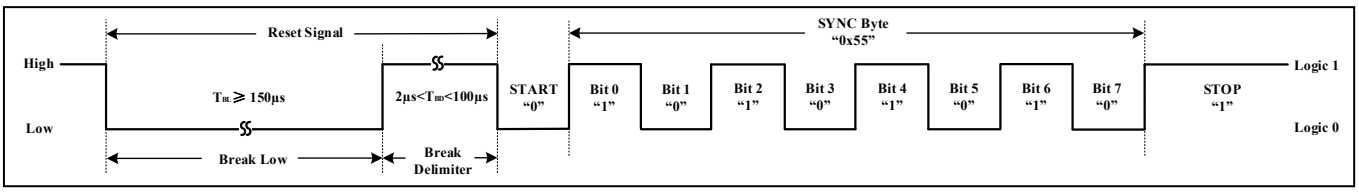


Figure 7 Bus Reset and SYNC Command

Break Low time (T_{BL}): min time 150μs

Break Delimiter time (T_{BD}): Greater than 2μs, max timeout 100μs

SYNC 0x55: The first SYNC bit length is decided by lowest baud-rate (>=100Kbps)

Before communication, the host needs to first send a bus reset comment to reset all slaves' Lumibus status.

Bus Reset IFG

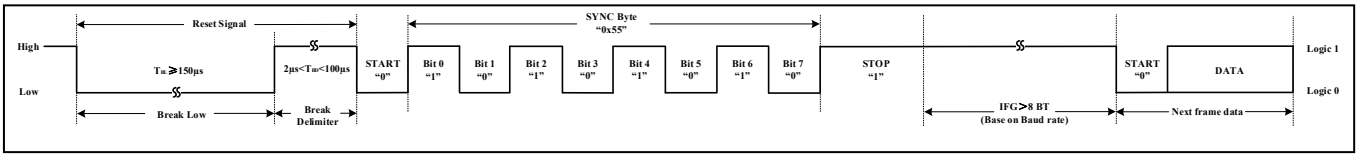


Figure 8 Bus Reset IFG (Single Device)

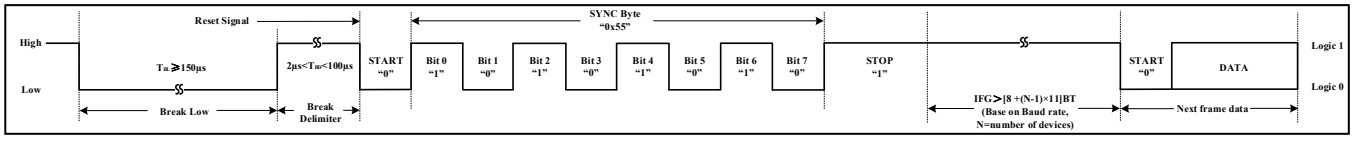
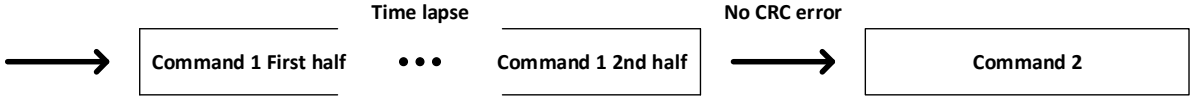


Figure 9 Bus Reset IFG (Cascade Application)

For host, it is necessary to waiting an IFG (Inter-Frame Gap) between sending the Bus Reset and next frame data. As shown in Figure 8 and Figure 9, the time of IFG need greater than 8bits baud rate,
or greater than [8+ (N-1) ×11] bits baud rate in cascade application, where N is the number of devices in a chain.

One complete UART frame can be received successfully even if the frame is not sent continuously. CRC error could be determined by reading back the written data byte.



If host's watch dog time is disabled or time laps is within watchdog time

Wakeup Operation

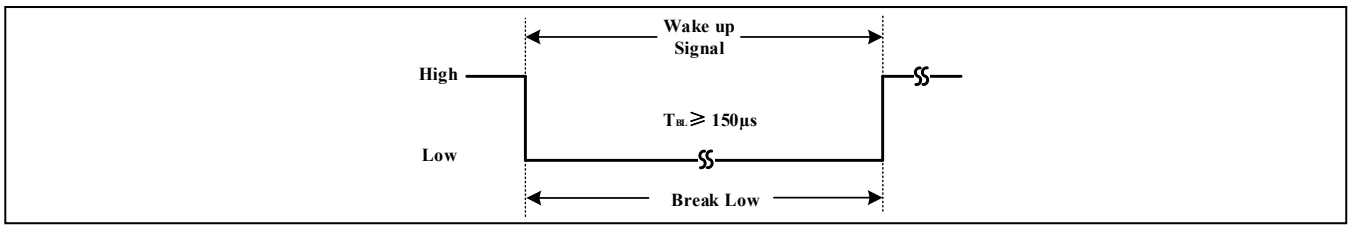


Figure 10 Wake up Signal

After IS32FL3202 enters power saving mode, it can be awakened by a break low signal ≥150μs.

Writing Operation

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Register Date Byte	N (1~16)
CRC Bytes	2
Total	N+5

Write Command Frame Structure (write: N = 1~16)

CMD Frame Header	Device ID	Register Start Address	N Bytes of Data	CRC_L	CRC_H
1 Byte	1 Byte	1 Byte	N Bytes	1 Byte	1 Byte

Reading Operation

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
CRC Bytes	2
Total	5

Read Command Frame Structure

CMD Frame Header	Device ID	Register Start Address	CRC_L	CRC_H
1 Byte	1 Byte	1 Byte	1 Byte	1 Byte

Response

Byte Types	Number of Bytes
RSP Frame Header Byte	1
Device ID Byte	1
Register Date Byte	N (1~16)
CRC Bytes	2
Total	N+4

Response Frame Structure

RSP Frame Header	Device ID	Register Data	CRC_L	CRC_H
1 Byte	1 Byte	N Bytes	1 Byte	1 Byte

Burst Read Command Format Structure

CMD Frame Header	Device ID	Register Start Address	CRC_L	CRC_H
0b1110xxxx	Address n	Start Register Address	CRC_L [7:0]	CRC_H [15:8]
1 Byte	1 Byte	1 Byte	1 Byte	1 Byte

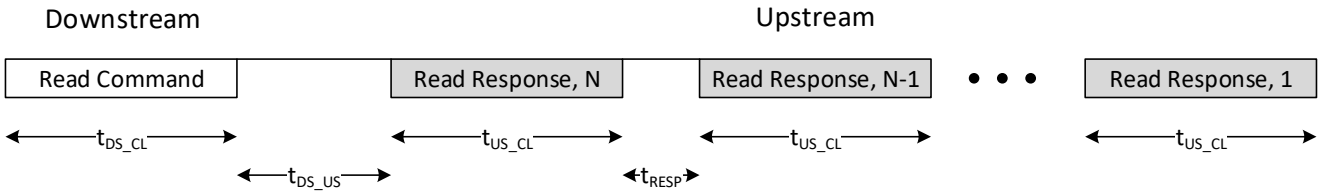
CMD Frame Header: 0b1110xxxx(0xEx), determines read data length,

Bit [3:0] = [0000] = 1 byte, …, Bit [3:0] = [1111] = 16 Bytes;

Device ID：Address n， n is the number of bursts read devices

CMD Frame Header lower 4 bits indicates the total number of bytes (1 – 16 bytes) and Reg Address indicates the starting address.

When the host issues the burst read command in broadcast mode, the host can read all register contents from device address #N (the last device) to #1 as shown in the following timing diagram. It starts from device #N, and with a time t_{DS_US} and t_{RESP} between devices for the next device read data, until the first device data is read. Note that when using this feature, device address must be assigned consecutively.



Where the t_{DS_US}>17bits (follow communication baud rate) and t_{RESP} >17bits (follow communication baud rate).

Special Command

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

Special Command Frame Structure

CMD Frame Header	Device ID	CRC_L	CRC_H
1 Byte	1 Byte	1 Byte	1 Byte

Please check the below CMD and RSP Frame Header for more information about the special command CMD Frame Header.

CMD and RSP Frame Header

	D7	D6	D5	D4	D3	D2	D1	D0
CMD Frame Header	FRM_TYPE =1	W/R	BCON	DATA[4:0]				
Response Frame Header	FRM_TYPE=0	-	-	-	RESP[3:0]			

CMD Frame Header

D7(FRM_TYPE): 0 = Response Frame;
1 = Command Frame;

D6(W/R): 0 = write;
1 = read;

D5(BCON): 0 = normal single device writes and read command;
1 = broadcast write and read command; When BCON = 1 and Device ID = FFh, broadcast to all devices;

D4~D0(DATA [4:0]): When DATA [4] =0: the DATA [3:0] determines transmit data length,
DATA [4:0] = [00000] = 1 byte, …, DATA [4:0] = [01111] = 16 Bytes;
When DATA [4] =1: the DATA [3:0] represents special write command, as below:

DATA [4:0] = [11100] PWM SYNC synchronization, works with broadcast mode to reset all slaves' PWM counters

DATA [4:0] = [11110] Registers reset command: to reset all function registers to default values (address 0x00~0x1D) when receiving this command (support both normal command and broadcast command);

DATA [4:0] = [11000] PWM data update latch command; PWM data is loaded upon when receiving this command (support both normal command and broadcast command);

Response Frame Header

D7(FRM_TYPE): 0 = Response Frame;
1 = Command Frame;
D6:D4 are reserved
D3~D0(RESP [3:0]): Response data length, RESP [3:0] = [0000] = 1 byte, …, RESP [3:0] = [1111] = 16 bytes;

Device ID Byte

Device ID [7:0]: Device address is assigned by LAA method

CRC Bytes

The host sends command to IS32FL3202 using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame data, e.g., CMD Frame Header, Device ID, Register Address, N Bytes of Data. Lower CRC byte first followed by higher CRC byte.

CMD Frame Header	Device ID	Register Start Address	N Bytes of Data	CRC_L	CRC_H
1 Byte	1 Byte	1 Byte	N Bytes	1 Byte	1 Byte

The following is a reference CRC checksum C code.

```
Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
{
        Uint16 crc = 0;
        Uint16 I;
        while (len--)
        {
                crc ^= *buf++;
                for (I = 0; I < 8; I++)
                {
                crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
                }
        }
        return crc;
}
```

When IS32FL3202 sends back CRC to the host, the data needs to be bit reversed then compare with the CRC data. The following is a reference CRC reverse bit checksum code.

```
Uint8 reverse_byte(Uint8 byte)
{
	// First, swap the nibbles
	byte = (((byte & 0xF0) >> 4) | ((byte & 0x0F) << 4));
	// Then, swap bit pairs
	byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
	// Finally, swap adjacent bits
	byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
	// We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
	return byte;
}
```

The following is a reference code for checking the returned data against CRC data.

```
bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
{
	Uint16 crc_calc; // Calculated CRC
	Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
	// Calculate the CRC based on bytes received
	crc_calc = crc_16_ibm(rx_buf, crc_start);
	crc_lsb = (crc_calc & 0x00FF);
	crc_msb = ((crc_calc >> 8) & 0x00FF);
	// Perform the bit reversal within each byte
	crc_msb = reverse_byte(crc_msb);
	crc_lsb = reverse_byte(crc_lsb);
	// Do they match?
	if((*(rx_buf + crc_start) == crc_lsb) && (*(rx_buf + crc_start + 1) == crc_msb))
	{
		return TRUE;
	}
	Else
	{
		return FALSE;
	}
}
```

LAA, Location Address Assignment

Location Address Assignment method (LAA) refers to the method that is used to automatically assign a unit address to the equally built slave devices, e.g., ISFL323202, that are located within a Lumibus system.LAA method is used in conjunction with Lumissil's proprietary bus, Lumibus as described earlier, that is a modification of CAN bus to take advantage of its well-established physical layer definition, as well as UART protocol, for its robust, chip-to-chip communication.

LAA Basic Function

Each IS32FL3202 device has a built-in LAA switch. The LAA line is routed through this built-in LAA switch of each Lumibus slave unit.

During normal operation, the LAA switch of the Lumibus slave unit is always closed. The only exception is during the LAA configuration process, when the LAA switch is opened to disconnect all following Lumibus slave units from the Lumibus bus communication.

The LAA configuration process starts with an LAA initialization command. This command causes all Lumibus slave units to reset the NAD (Network Address) and open their respective LAA switch. As a consequence, the first Lumibus slave unit (next to the Lumibus master) is the only Lumibus slave unit that can still receive LAA commands. Thus, the following NAD assignment command will be solely received by the first LAA slave unit. When the NAD command has been correct, the new NAD will be accepted and the LAA switch will be closed to enable the following Lumibus slave unit to receive LAA messages. Thus, with the next NAD assignment command the following unassigned Lumibus slave unit will be assigned with a new NAD and afterwards also closes its LAA switch. This procedure continues until all Lumibus slave units are assigned with its dedicated NAD. Afterwards all LAA switches are closed and a command is sent to inform all Lumibus slave units about the LAA process closure. In the following section "Configuration Flow" further details how the LAA configuration process are provided.

The following system block diagram shows the LAA configuration flow (write), as well as SNPD read back flow. Normal data follows the same data flow.

LAA Configuration Flow

The LAA uses five LAA node configuration services. They are distinguished via SNPD sub functions. The LAA node configuration services are listed in Table 1.

Table 1 LAA SNPD Sub Functions

SNPD Sub Function	Service Description
LAA Initialization	Starts LAA configuration process
LAA NAD Assignment	Assigns LAA slave with new NAD
LAA Finished	Informs about LAA configuration process closure
LAA read NAD register	Read out NAD from OTP content NAD register
LAA write NAD to OTP NVM	Write new NAD to OTP NVM register
LAA read from OTP NVM	Read out NAD From OTP NVM register

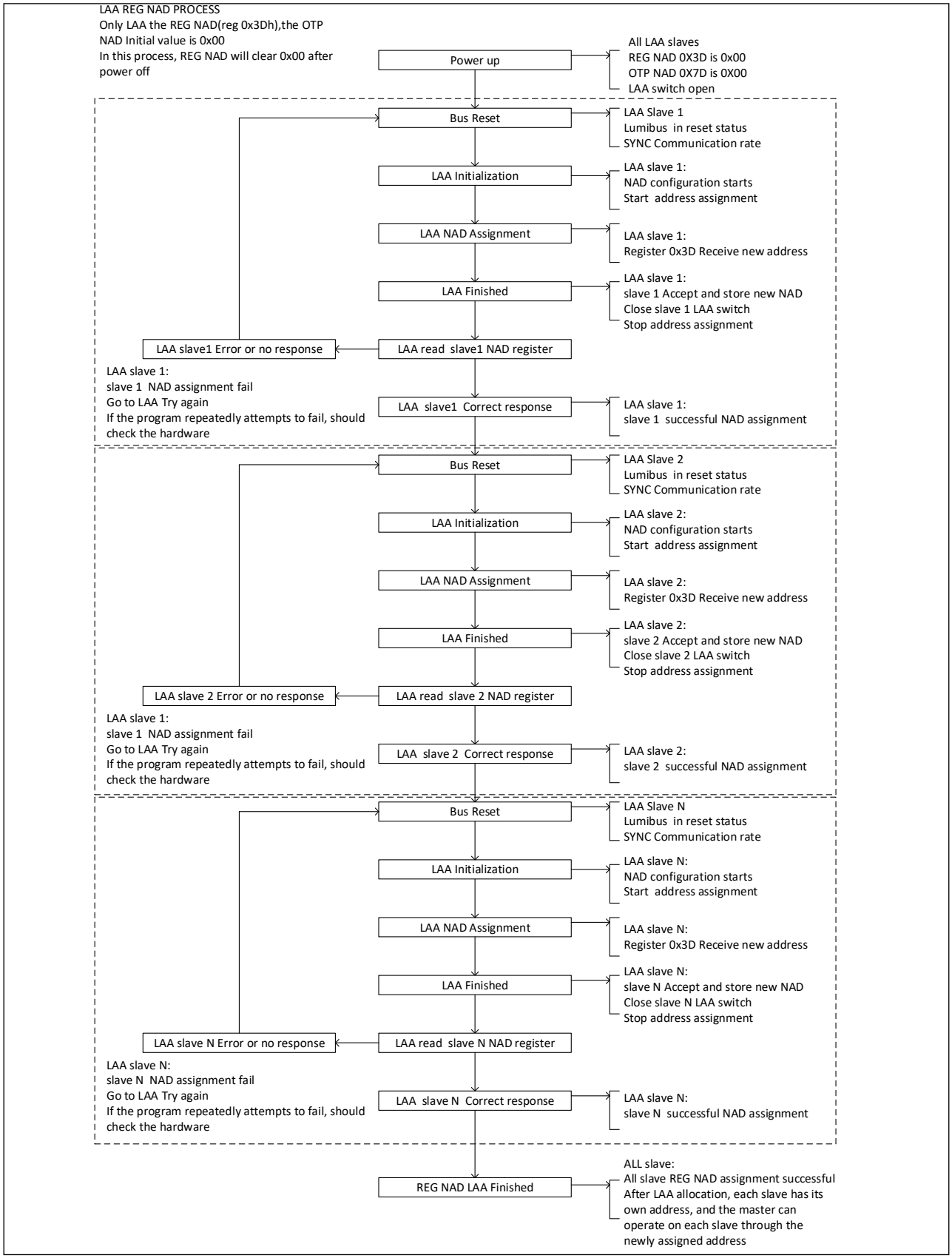


Figure 11a LAA SNPD Configuration Flow (LAA REG NAD PROCESS)

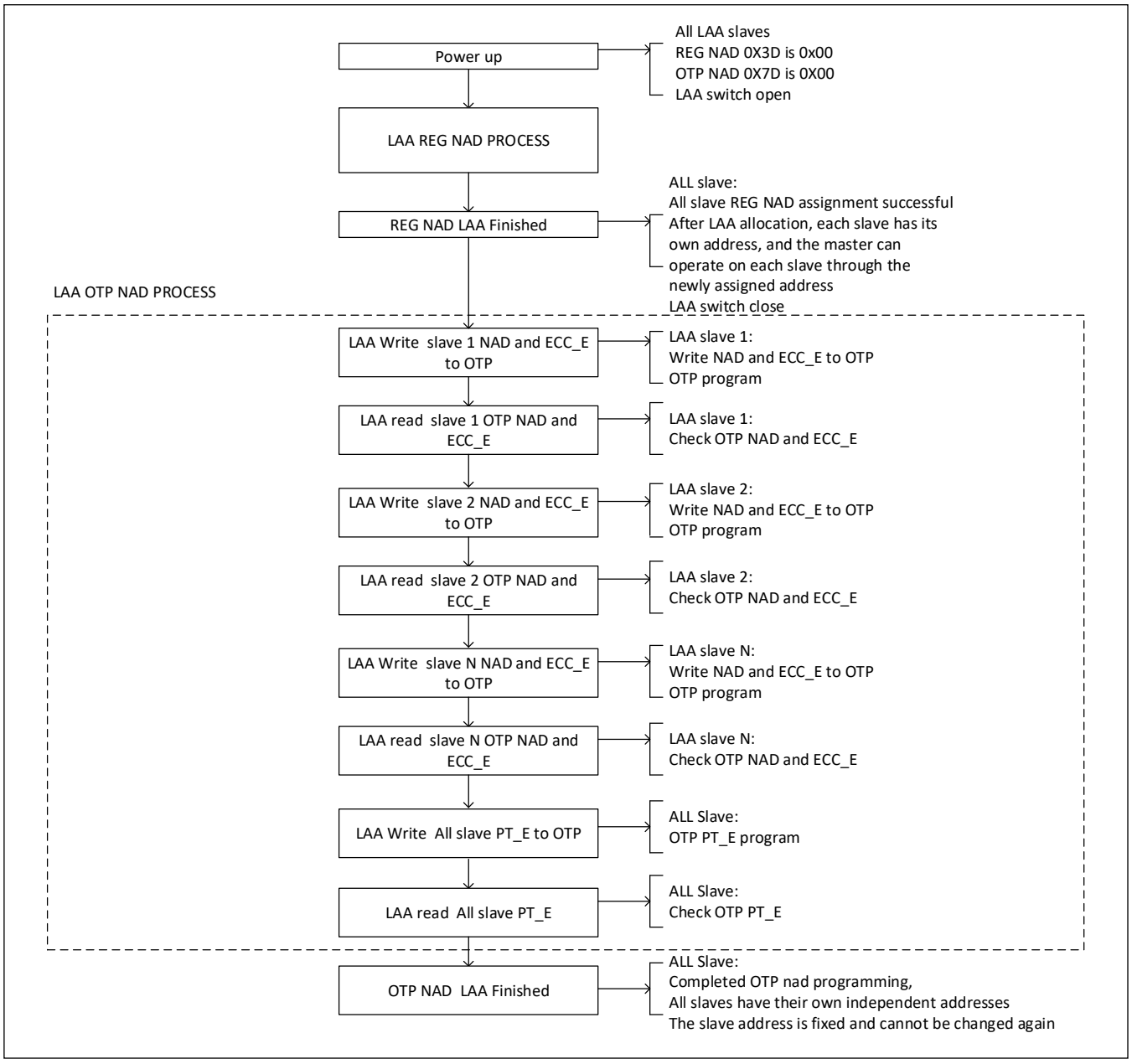


Figure 11b LAA SNPD configuration flow (LAA OTP NAD PROCESS)

Figure 11a and 11b illustrate the LAA configuration flow, which reflects a more detailed explanation in terms of the timing relationship of the flow. Its corresponding commands are shown in Table 1. The LAA process is framed with a starting and a ceasing service. The LAA SNPD sub function LAA Initialization starts the configuration and causes all LAA slave units to open their LAA switch. The LAA process closure is communicated with the LAA SNPD sub function LAA Finished.

With the LAA SNPD sub function LAA NAD Assignment an LAA slave unit is allocated with a dedicated NAD. The NAD will be accepted only, if the LAA slave unit has not been assigned with a new NAD, yet, and the LAA switch is still open. After NAD acceptance, the LAA switch is closed. LAA NAD Assignment is ignored from already assigned LAA slave units.

In order to check whether the new NAD has been accepted, the Lumibus master can optionally request acknowledgment from the last assigned LAA slave unit by means of a positive Lumibus slave response. This approach bases on a handshake principle.

LAA NAD Assignment is sent to each LAA slave unit, respectively, until all LAA slave units have been assigned with a new NAD according to the installation location. When all LAA slave units have accepted a new NAD, then all LAA switches are closed again.

During LAA configuration the SNPD sub function LAA NAD assignment shall be accepted from unassigned LAA slaves only, i.e., all LAA slaves with assigned new NAD will ignore this SNPD sub function. Thus the first Lumibus slave closed the LAA switch and shall ignore any further LAA NAD assignment and the second Lumibus slave can receive Lumibus frames from the Lumibus master and shall accept a valid LAA NAD assignment. After successful assignment of new NAD, the second Lumibus slave shall also close its LAA switch and consequently enable the next Lumibus slave in the daisy chain for LAA assignment.

With this configuration flow each LAA slave will be assigned one by one with a new NAD, typically starting from 1 and assigned in an ascending order. Note that the SNPD process for all LAA slaves (from reception of LAA Initialization until reception of LAA Finished) shall be completed within 4s, because when Lumibus inactivity is detected an LAA slave shall close the LAA switch and enter bus sleep mode.

In the above flow, the assigned address, NAD, to each slave will be permanently stored in OTP. This flow's advantage is that after out of factory, the NAD of each slave is assigned and fixed; the system does not need to assign NAD to each slave every time during power up. The disadvantage is that in case there is any one, or more, slave that is broken and is replaced, the NAD flow needs to be executed once again in the shop to re-assign this NAD.

Alternatively, this LAA flow can be execute every time when the system is powered up; NAD is not stored in OTP. The NAD of each slave each time is assigned automatically but it will take longer initialization time, especially if there are many slaves in the chain and in the system.

LAA Initialization Command

Host needs to first send this LAA Initialization command before any LAA NAD Assignment action. After IS32FL3202 receives this LAA Initialization command, register 0x3D then can use LAA NAD Assignment command for NAD assignment.

CMD Frame Header	Device ID	Register Address	CNAD	LDAT	CRC_L	CRC_H
0xA1	0xFF	0xAC	0x7F	0x01	0xAC	0x1C

LAA NAD Assignment Command

LAA NAD assignment command is to change register 0x3D for new NAD address.

CMD Frame Header	Device ID	Register Address	Register Data	CRC_L	CRC_H
0x80	iNAD	0x3D	NAD	1 Byte	1 Byte

Where iNAD is current NAD stored in 0x3D (Initial value = 0x00), NAD is the target new address.

LAA NAD Finished Command

After completing LAA NAD Assignment Command to change IS32FL3202 NAD address, host needs to send this LAA NAD Finished Command to complete NAD assignment action. After receiving LAA NAD Finished Command，LAA NAD Assignment will become inactive, and will become active again only upon receiving another LAA Initialization Command.

CMD Frame Header	Device ID	Register Address	CNAD	LDAT	CRC_L	CRC_H
0xA1	0xFF	0xAC	0x7F	0x03	0x2D	0xDD

LAA read NAD register

Read 0x3D register to obtain current NAD:

CMD Frame Header	Device ID	Register Address	CRC_L	CRC_H
0xC0	iNAD	0x3D	1 Byte	1 Byte

Where iNAD is current NAD stored in 0x3D (Initial value = 0x00), and iNAD becomes the target new address after LAA.

Response:

RSP Frame Header	Device ID	Register Data	CRC_L	CRC_H
0x00	iNAD	1Byte	1 Byte	1 Byte

RSP Frame Header: 0x00 is read data length

Device ID: iNAD is current NAD stored in 0x3D (Initial value = 0x00), and iNAD becomes the target new address after LAA

Register Data: the data of 0x3D register

LAA: Write NAD to OTP

CMD Frame Header	Device ID	Register Address	Data of 0x7D Register	Data of 0x7E Register	CRC_L	CRC_H
0x81	iNAD	0x7D	NAD	ECC_E	1 Byte	1 Byte

No write operation if (iNAD=0 or iNAD !=NAD or ECC_error)

CMD Frame Header	Device ID	Register Address	Data of 0x7D Register	Data of 0x7E Register	Data of 0x7F Register	CRC_L	CRC_H
0x82	iNAD	0x7D	NAD	ECC_E	PT_E	1 Byte	1 Byte

The difference between 0x81 and 0x82 is that in 0x82, protect bit status is written into OTP while in 0x81, this bit is not written into OTP.
If iNAD = 0, or iNAD is not the current value, or when there is ECC error, the data will not be written into OTP.

LAA: Read NAD and ECC from OTP

CMD Frame Header	Device ID	Register Address	CRC_L	CRC_H
0xC1	iNAD	0x7D	1 Byte	1 Byte

Response NAD and ECC from OTP

RSP Frame Header	Device ID	NAD Register(0x7D) Data	ECC Register(0x7E) Data	CRC_L	CRC_H
0x01	iNAD	1Byte	1Byte	1 Byte	1 Byte

RSP Frame Header: 0x01 is read data length

Device ID: iNAD is current NAD stored in 0x7D (Initial value = 0x00), and iNAD becomes the target new address after LAA

Register Data: the data of 0x7D and 0x7E register

LAA: Read NAD, ECC and PT_C from OTP

CMD Frame Header	Device ID	Register Address	CRC_L	CRC_H
0xC2	iNAD	0x7D	1 Byte	1 Byte

The difference between 0xC1 and 0xC2 is that in 0xC2, protect bit status is read back while in 0xC1, this bit is not included.

Response NAD, ECC and PT_C from OTP

RSP Frame Header	Device ID	NAD Register (0x7D) Data	ECC Register (0x7E) Data	ECC Register (0x7F) Data	CRC_L	CRC_H
0x02	iNAD	1Byte	1Byte	1Byte	1 Byte	1 Byte

RSP Frame Header: 0x02 is read data length

Device ID: iNAD is current NAD stored in 0x7D (Initial value = 0x00), and iNAD becomes the target new address after LAA

Register Data: the data of 0x7D, 0x7E and 0x7F register

OTP COMMAND FRAME

OTP Write Frame (Write to OTP Content Register: 0x29~0x3F)

CMD Frame Header	Device ID	Register Start Address	N Bytes of Data	CRC_L	CRC_H
0b100{N}	1 Byte	1 Byte	N Bytes	1 Byte	1 Byte

OTP Read Frame (Read from Content Register: 0x29~0x3F)

CMD Frame Header	Device ID	Register Start Address	CRC_L	CRC_H
0b110{N}	1 Byte	1 Byte	1 Byte	1 Byte

OTP Content Register Response Frame

RSP Frame Header	Device ID	N Bytes of Data	CRC_L	CRC_H
0b000{N}	1 Byte	N Bytes	1 Byte	1 Byte

OTP Write Frame (Write to OTP NVM Register: 0x69~0x7F)

CMD Frame Header	Device ID	Register Start Address	N Bytes of Data	CRC_L	CRC_H
0b100{N}	1 Byte	1 Byte	N Bytes	1 Byte	1 Byte

OTP Read Frame (Read from OTP NVM Register: 0x69~0x7F)

CMD Frame Header	Device ID	Register Start Address	CRC_L	CRC_H
0b110{N}	1 Byte	1 Byte	1 Byte	1 Byte

OTP NVM Register Response Frame

RSP Frame Header	Device ID	N Bytes of Data	CRC_L	CRC_H
0b000{N}	1 Byte	N Bytes	1 Byte	1 Byte

OTP program sequence timing

The OTP Zone C, Zone D and Zone E bits are set to 0 when freshly out of factory. Bits may be set during the programming cycle, which is no longer erasable. Regardless of the status of the bits. Once the Fuse-Protection bit is programmed to 1, The OTP content is no longer programmable.

Programming any bit of the OTP memory is executed by issuing the program command. During the whole programming procedure, an external programming voltage of 4.6V~4.8V must be applied to the PGM pin. The actual programming sequence is fully self-controlled by the device.

During the binning programming data to Zone C, the OTP NVM Zone C registers (29h~35h) data must the same as OTP content Zone C registers data (69h~75h).

During the binning programming data to Zone D, the OTP NVM Zone D registers (36h~3Ch) data must the same as OTP content Zone D registers data (76h~7Ch).

During the binning programming data to Zone E, it must complete the LAA (Location Address Assignment) process first before writing the OTP in Zone E.

ECC register is the verification of data written to OTP, the data will not be written into OTP when ECC error.

The programming procedure takes some time. Depending on the number of bits to be programmed to logic 1 and programming each digit requires at least 0.5ms Typ., it is required to wait an appropriate time before issuing the next command. The programming procedure cannot be interrupted. If another command is issued too early, it gets ignored.

LED CALIBRATION

LED Calibration Background

The visual color depends on the wavelength of the light emitting device, as shown in Figure 12. The Dominant Wavelength of an LED is the wavelength of the photons that an LED emits the vast majority of the time. When use R, G, B LED's as a color light source, its color characteristic is measured by color temperature (per the CIE standard, color temperature is a rating of a light source's color output). To calibrate a color LED dot, D75 and D65 are commonly used as reference. D75 (7500K) is a bluish colored light source originally used for grading cotton and other evaluation applications. It has been replaced by D65 as the standard source for these applications. It accentuates blue and subdues green and red and is derived from the light coming in a north facing window in the northern hemisphere at noon at various times throughout the year. D65 (6500K) is a light bluish colored light source used in color matching applications of paints, plastics, textiles, raw inks, and other manufactured products. It is the only daylight source that was actually measured.

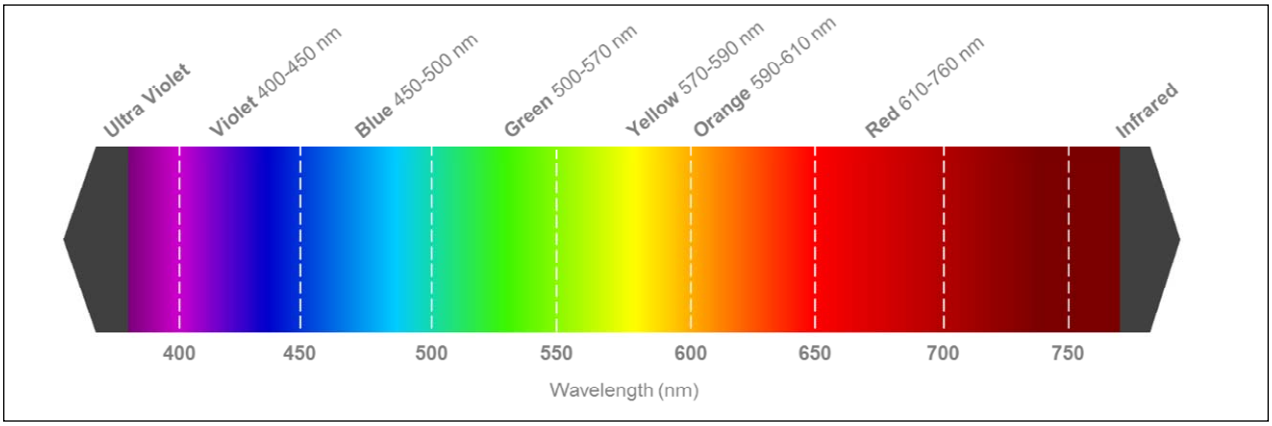


Figure 12 Color spectrum

The dependence of a typical LED wavelength and its bias current is shown in Figure 13, left, using a green LED as an example. The LED wavelength, in turn, can impact the output luminance as shown in Figure 13, right, which shows that the light intensity is a function of wavelength and its bias current. By adjusting the LED bias current, the dominant wavelength can be adjusted to its desirable target value.

While this relationship is similar for LED's manufactured among all LED manufacturers, their dependence varies from manufacture to manufacturer, from lot to lot and from die to die, even if the same process flow is used. Traditionally, LED manufactures separate LED's into many different bins per their optical characteristics. This creates logistic complexity for the LED manufacturers as well as end customers. It is desirable for the LED driver/controller to calibrate each controlled color LED for a perfect color presentation using an efficient production flow, with the calibrated parameters stored permanently in a non-volatile memory inside the color LED package.

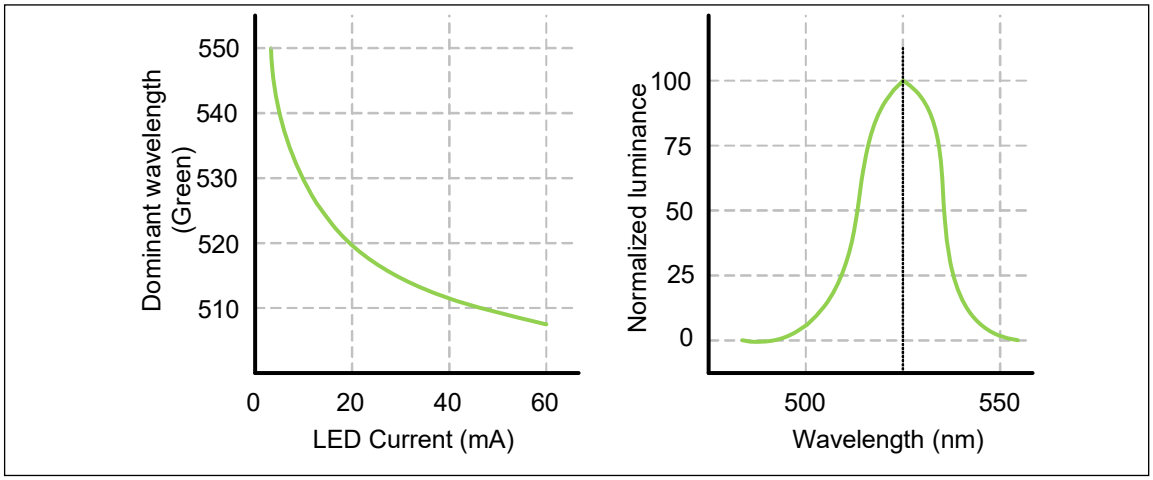


Figure 13 Wavelength and luminance output dependence of LED current

Note 8: Luminance is the luminous intensity, projected on a given area and direction. Luminance is an objectively measurable attribute. The unit is "Candela per Square Meter" (cd/m2). Brightness is a subjective attribute of light. The monitor can be adjusted to a level of light between very dim and very bright. Brightness is perceived and cannot be measured objectively. They are used interchangeably in this document.

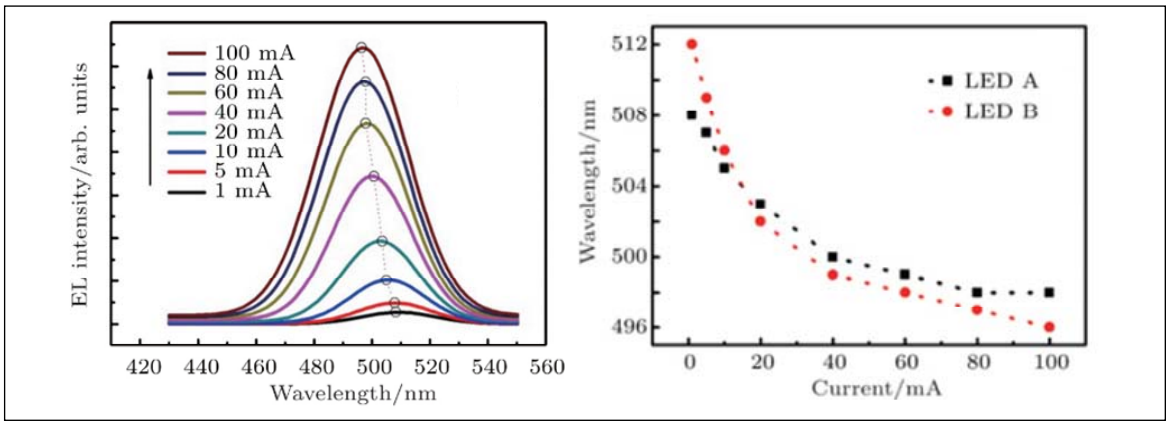


Figure 14 Luminance intensity vs. bias current

Wavelength is also a weak function of bias current as shown in Figure 14 from literature. Therefore, once the bias current is fixed, adjusting intensity should be completely based on adjusting PWM duty cycle.

IS32FL3202 can support this color calibration for replacing the cumbersome binning process. After the color calibration is fixed with calibrated values in the on-die OTP, end users need only to control output brightness by the 12-bit PWM method.

Color Calibration Flow

In IS32FL3202, each LED channel can drive up to 63mA current. Each channel current can be controlled by a 6-bit DC registers for 64 levels of maximum reference current (DC_max). D65 can be used as color reference to obtain its corresponding red, green and blue dominant wavelengths as initial values, which in turn can derive their corresponding current by adjusting their DC register and PWM register.

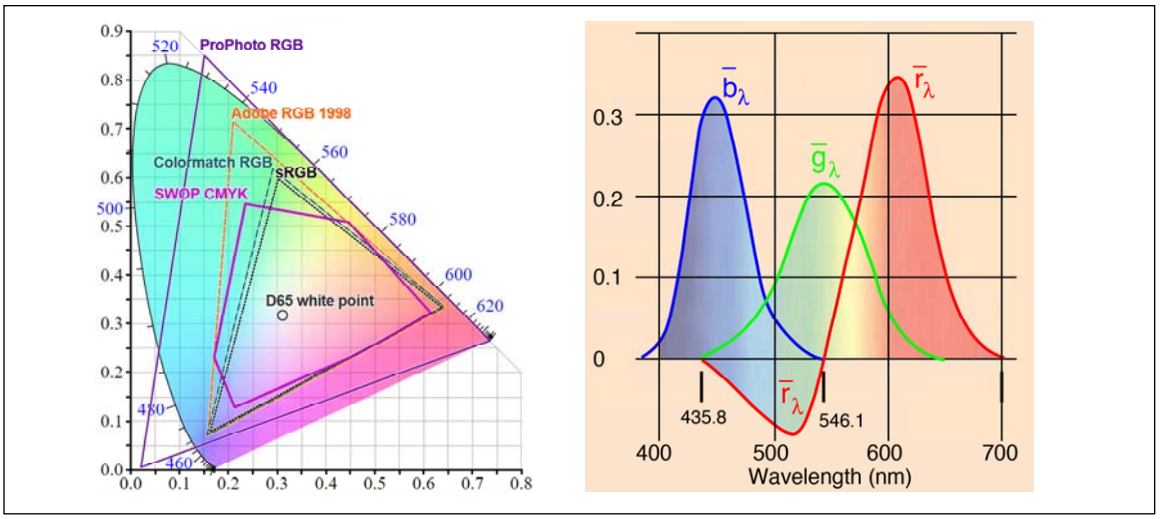


Figure 15 Color calibration R, G, B initial value setting using D65 (daylight white) wavelength as reference. Power spectral will be adjusted by R, G, B PWM_CAL register values. Optical calibration is carried out by optical equipment during production.

As shown in Figure 15, after the parameter of R, G and B is fixed, the power spectral of D65 white light for IS32FL3202 is calibrated by adjusting PWM_CAL register value (of R, G, and B).

TEMPERATURE COMPENSATION

Temperature Compensation Background

A typical temperature dependence of LED color is shown in Figure 16. LED color, in particular, the red LED, is known a nearly linear function of its junction temperature. When the operating temperature is changed, the LED color is shifted. Correction of this temperature dependence is particularly of interest for the automotive ambient light application where the vehicle can operate over a wide temperature range.

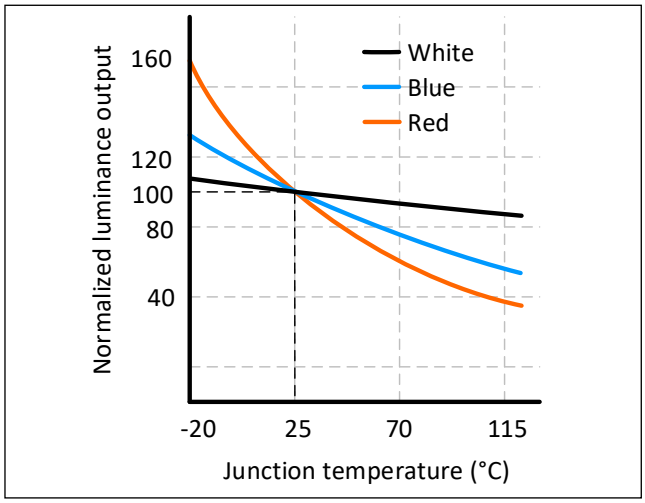


Figure 16 Temperature Dependence of LED Color

Temperature Compensation Method

Luminance of LED is a function of junction temperature, as shown in Figure 17, left. To maintain the same luminance to compensate for this temperature dependence, the PWM slope can be adjusted accordingly, as shown in Figure 17, right. The amount of adjustment will depend on the junction temperature, which is measured periodically by the on-die temperature sensor. The temperature compensation takes place automatically based on the sensed temperature at the PWM cycle boundary. The luminance-temperature dependence varies from manufacturer to manufacturer but is assumed fixed and linear for the same process.

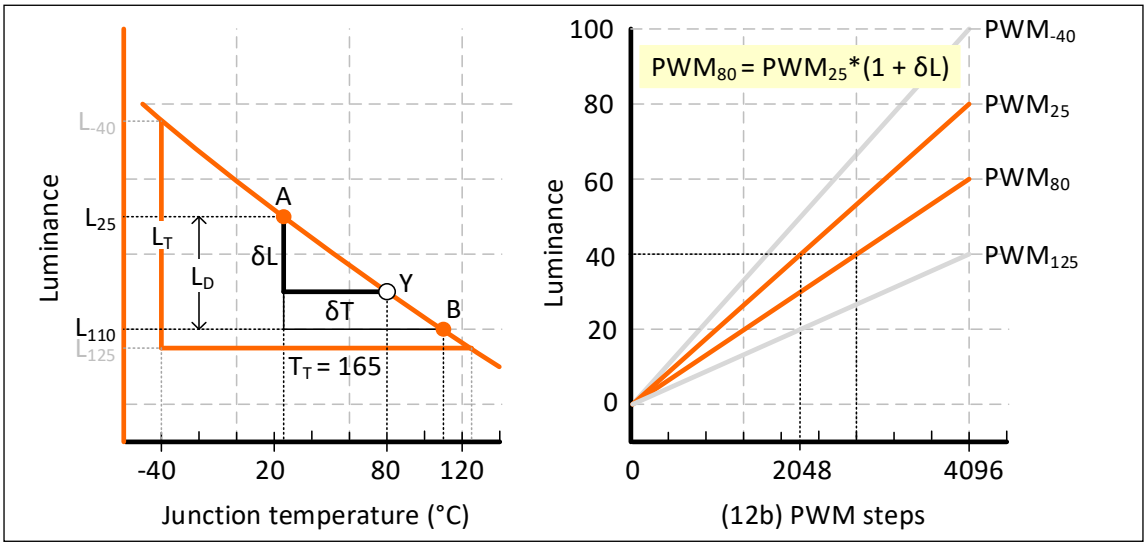


Figure 17 Temperature Compensation Theory

Temperature Compensation Calibration

Calibration of IS32FL3202 consists of 2 steps: electrical calibration and optical calibration.

Electrical calibration is performed by Lumissil, while optical calibration is performed by LED maker that can provide optical measurement in production, optical calibration flow is shown in Figure 18. Lumissil can provide screened good dies with calibrated data, that is stored in the on-die OTP.

After both calibration data flows are performed, the calibrated electrical and optical data is stored in on-die OTP. the finished IS32FL3202 is shipped to end module customer for module assembly. The only uncommitted item is the SNPD address data, which is committed after LAA SNPD flow by storing NAD in the on-die OTP.

End customer only needs to provide operation R, G, B 12-bit PWM data for various lighting effect, without worrying about the LED color and temperature variation.

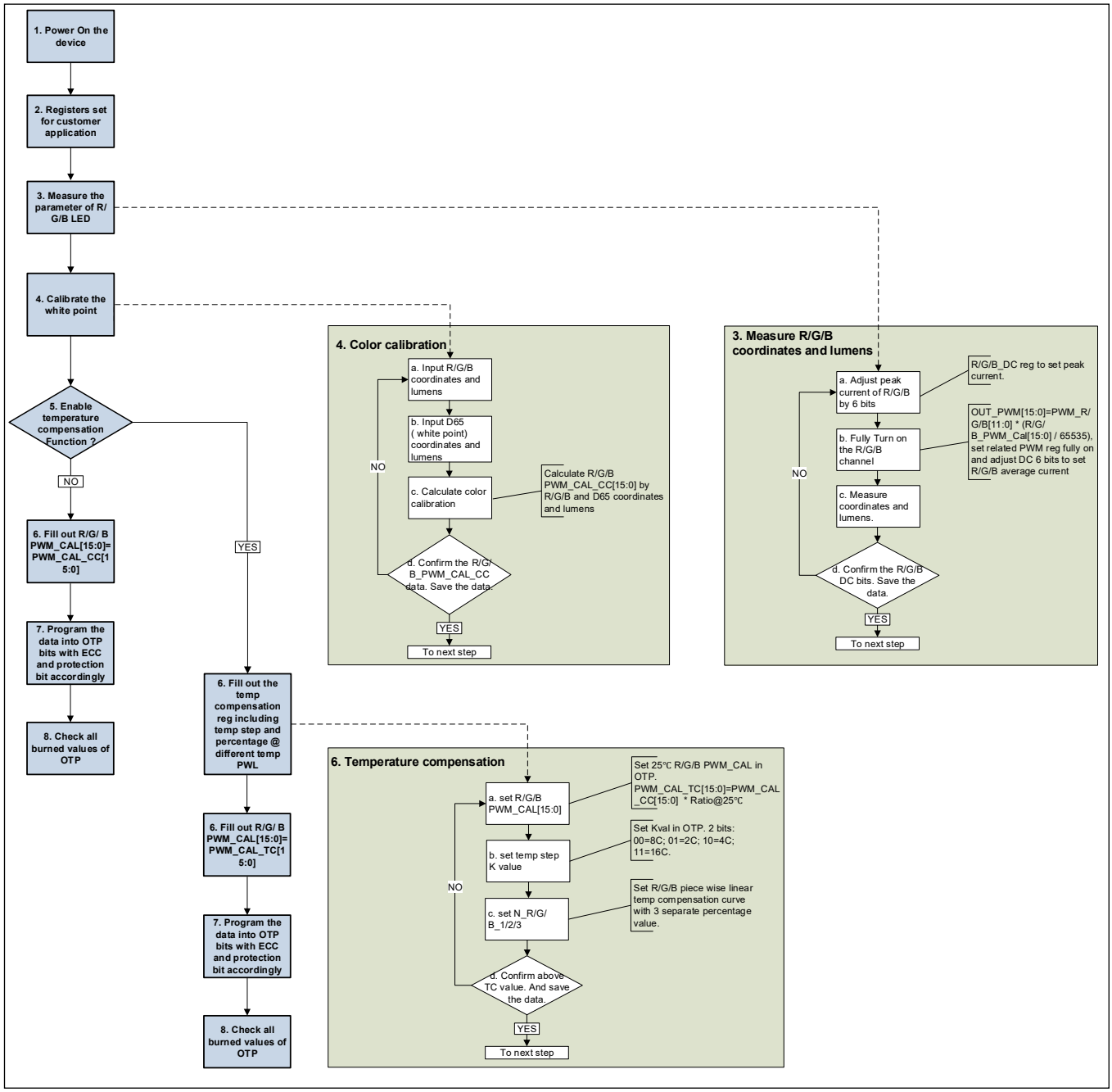


Figure 18 Optical calibration flow chart

REGISTER MAPPING

Table 2 Function Register Definitions

Address	Name	Function	R/W	Table	Default
01h	OUTR PWM Register 1	Set OUTR PWM Register 1	R/W	5	0000 0000
02h	OUTG PWM Register 1	Set OUTG PWM Register 1	R/W	5	0000 0000
03h	OUTB PWM Register 1	Set OUTB PWM Register 1	R/W	5	0000 0000
04h	OUTR PWM Register 2	Set OUTR PWM Register 2	R/W	5	0000 0000
05h	OUTG PWM Register 2	Set OUTG PWM Register 2	R/W	5	0000 0000
06h	OUTB PWM Register 2	Set OUTB PWM Register 2	R/W	5	0000 0000
07h	Control Register 2	Second general control register	R/W	6	xx00 x110
08h	Control Register 1	First general control register	R/W	7	x001 x000
09h	Communications Watchdog Timer Register	Set Communications Watchdog	R/W	8	0100 0100
0Ah	ADC Control Register	ADC Control register	R/W	9	x000 0000
0Bh	ADC Enable and Sample Hold Register	ADC Sample Hold Register	R/W	10	xx00 0000
0Ch	ADC Data Register ADCR1H High 8 bits	Read back ADC result for cycle sampling (High 8 bits)	R	11	0000 0000
0Dh	ADC Data Register ADCR1L Low 4 bits	Read back ADC result for cycle sampling (Low 4 bits)	R	12	0000 0000
0Eh	ADC Data Register ADCR2H High 8 bits	Read back ADC result for single sampling (High 8 bits)	R	13	0000 0000
0Fh	ADC Data Register ADCR2L Low 4 bits	Read back ADC result for single sampling (Low 4 bits)	R	14	0000 0000
10h	Fault Flag register	Fault flag register	R	15	0000 0000
11h	Open and Short Register	Store the open and short information of LED	R	16	0000 0000
12h	CRC Error Count	CRC Error Status Count	R/W	17	0000 0000
14h~15h	OUTR Output PWM Duty	Store final 16bits PWM output values for OUTR	R	18/19	0000 0000
16h~17h	OUTG Output PWM Duty	Store final 16bits PWM output values for OUTG	R	20/21	0000 0000
18h~19h	OUTB Output PWM Duty	Store final 16bits PWM output values for OUTB	R	22/23	0000 0000
1Ch	Baud rate Control Register 1	Set communications baud rate	R/W	24	000x xx00
1Dh	Baud rate Control Register 2	Set communications baud rate	R/W	25	0000 0000
40h	OTP Status Register	Store OTP write status	R	26	0000 0010
41h	ECC Status Register 1	Store 1bit ECC error status	R	27	0000 0000
42h	ECC Status Register 2	Store 2bits ECC error status	R	28	0000 0000

Table 3 OTP Content Register Definitions

Address	Name	Function	R/W	Table	Default
29h~2Fh	Temperature compensation configuration register	Set temperature compensation step and percentage	R/W	29	0000 0000
30h~32h	OUTR/G/B Channels Output Current and VF Reference register	Set OUTR/G/B Channels Output Current and VF Reference	R/W	30	0000 0000
33h	VF ADC value at Room Temperature Register	Set VF ADC value at Room Temperature	R/W	31	0000 0000
34h	ECC Data of C Zone Register	ECC Data of C Zone	R/W	32	0000 0000
35h	Protect bit of C Zone Register	Protect bit of C Zone	R/W	33	0000 0000
36h~37h	OUTR PWM Output Calibration Register	Set 16 bits to calibrate OUTR PWM Output	R/W	34	0000 0000
38h~39h	OUTG PWM Output Calibration Register	Set 16 bits to calibrate OUTG PWM Output	R/W	34	0000 0000
3Ah~3Bh	OUTB PWM Output Calibration Register	Set 16 bits to calibrate OUTB PWM Output	R/W	34	0000 0000
3Ch	ECC Data and Protect bit of D Zone Register	ECC Data and protect bit of D Zone	R/W	35	0000 0000
3Dh	NAD Register	Store device address	R/W	36	0000 0000
3Eh	ECC Data of E Zone Register	ECC Data of E Zone	R/W	37	0000 0000
3Fh	Protect bit of E Zone Register	Protect bit of E Zone	R/W	38	0000 0000

Table 4 OTP NVM Register Definitions

Address	Name	Function	R/W	Table	Default
69h~6Fh	Temperature compensation configuration register	Set temperature compensation step and percentage	R/W	39	0000 0000
70h~72h	OUTR/G/B Channels Output Current and VF Reference register	Set OUTR/G/B Channels Output Current and VF Reference	R/W	40	0000 0000
73h	VF ADC value at Room Temperature Register	Set VF ADC value at Room Temperature	R/W	41	0000 0000
74h	ECC Data of C Zone Register	ECC Data of C Zone	R/W	42	0000 0000
75h	Protect bit of C Zone Register	Protect bit of C Zone	R/W	43	0000 0000
76h~77h	OUTR PWM Output Calibration Register	Set 16 bits to calibrate OUTR PWM Output	R/W	44	0000 0000
78h~79h	OUTG PWM Output Calibration Register	Set 16 bits to calibrate OUTG PWM Output	R/W	44	0000 0000
7Ah~7Bh	OUTB PWM Output Calibration Register	Set 16 bits to calibrate OUTB PWM Output	R/W	44	0000 0000
7Ch	ECC Data and Protect bit of D Zone Register	ECC Data and protect bit of D Zone	R/W	45	0000 0000
7Dh	NAD Register	Store device address	R/W	46	0000 0000
7Eh	ECC Data of E Zone Register	ECC Data of E Zone	R/W	47	0000 0000
7Fh	Protect bit of E Zone Register	Protect bit of E Zone	R/W	48	0000 0000

Function Register Definitions

Table 5 01h ~ 06h PWM Register

Channel	PWM Register 1	PWM Register 2
OUTR	01h	04h
OUTG	02h	05h
OUTB	03h	06h

There are 6 PWM Registers. Register 04h (PWMR2) and 01h (PWMR1) are used together to define OUTR channel PWM data. Register 04h (PWMR2) defines its higher 8 bits PWM data while register 01h (PWMR1) defines its lower 4 bits PWM data. Similarly, registers 05h (PWMG2) and 02h (PWMG1) are used together to define OUTG channel PWM data, while registers 06h (PWMB2) and 03h (PWMB1) are used together to define OUTB channel PWM data.

In the Control Register 2 (07h), bits 5 and 4 are defined as PWM_WIDTH, which has 4 PWM mode settings. When PWM_WIDTH setting is 00 (default), PWM Registers serve as one field PWM mode for channels R, G and B. This is the typical PWM data definition widely used by LED controller makers.

IS32FL3202 supports a unique, two field 12-bit PWM mode, defined by PWM_WIDTH of 01, 10 or 11. Two field PWM mode is explained shortly.

PWM_ WIDTH = 00: One Field PWM mode

01h (PWMR1), 02h (PWMG1), 03h (PWMB1)

Bit	D7	D6	D5	D4	D3	D2	D1	B0
Name					PWM Low 4 bits			
Default	0	0	0	0	0	0	0	0

04h (PWMR2), 05h (PWMG2), 06h (PWMB2)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWM High 8 bits							
Default	0	0	0	0	0	0	0	0

Registers 04h, 05h and 06h are to store the high 8 bits PWM content while registers 01h, 02h and 03h are to store the low 4 bits PWM content. 01h (low 4 bits) and 04h (high 8 bits) are 12 bits PWM data for R channel; likewise, 02h and 05h are 12 bits PWM data for G channel and 03h and 06h are 12 bits PWM data for B channel. Each LED current is modulated in 4096 steps.

PWM data for PWM Registers are supplied by the system host, and are updated only at the PWM cycle boundary.

The maximum current of each channel, I_{OUT}, that is obtained from OTP and the value of the PWM Registers decide the average current of each LED channel.

PWM_ WIDTH = 01, 10, 11: Two Field PWM mode

When PWM_ WIDTH = 01, 10 or 11, the PWM registers are divided into two fields. In the following discussion, PWMx1 and PWMx2 are used as these two fields, where x = R, G, or B. This mode can be used conveniently and flexibly for applications where chromaticity and luminance can be operated independently.

PWM_ WIDTH = 01

01h (PWMR1), 02h (PWMG1), 03h (PWMB1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-				PWMx1 4 bits			
Default	0	0	0	0	0	0	0	0

04h (PWMR2), 05h (PWMG2), 06h (PWMB2)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWMx2 8 bits							
Default	0	0	0	0	0	0	0	0

Definition of PWM_WIDTH = 01 will be discussed first. The other two definitions, 10 and 11, can be similarly understood and will be discussed later.

When PWM_WIDTH = 01, 12 bits PWM data is divided into 4 bits and 8 bits data registers for color and luminance data. Register 01h (PWMR1) can be used as 4 bits color definition (16 different colors can be specified), while register 04h (PWMR2) can be used as their corresponding 8 bits luminance definition (256 different luminance levels can be specified), i.e., 256 levels of luminance intensity level of each of these 16 colors can be described by these two fields. Register 02h (PWMG1) and register 03h (PWMB1) can be used as the other two sets of 4 bits color definition, while register 05h (PWMG2) and register 06h (PWMB2) can be used as the other two sets of 8 bits luminance definition.

Combining 01h, 02h and 03h together, there will be total of 16*16*16 = 4,096 colors specified by PWMx1 (x = R, G, B – each contributes 4 bits color data). When using this for ambient light application such as dimming function with fixed color, users can change luminance data (03h, 04h and 05h) by the host command at specified timing interval without changing LED color. Note that for this dimming function, registers 03h, 04h and 05h will have to be changed by the same value, or else the color will also change. The maximum dimming rate of the whole system will depend on the total number of IS32FL3202 on the Lumibus, which has a fixed maximum of 2Mbps total bandwidth.

Another ambient light function, cross fading, can also be implemented by this two field PWM mode. In this application, users can gradually change from the initial color (01h, 02h and 03h) to the targeted color over specified timing interval, with or without fixing the luminance data (04h, 05h, 06h). Again, the maximum cross fading rate of the whole system will depend on the total number of 3202 on the Lumibus.

Internally, the maximum PWM output value will be 15×255 = 3,825.

PWM_ WIDTH = 10

01h (PWMR1), 02h (PWMG1), 03h (PWMB1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	PWMx1 5 bits				
Default	0	0	0	0	0	0	0	0

04h (PWMR2), 05h (PWMG2), 06h (PWMB2)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	PWMx2 7 bits						
Default	0	0	0	0	0	0	0	0

When PWM_ WIDTH =10: 12 bits PWM data is divided into 5 bits and 7 bits data registers for color and luminance data.

The maximum PWM output value will be 31×127 = 3,937.

PWM_ WIDTH = 11

01h (PWMR1), 02h (PWMG1), 03h (PWMB1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	PWMx1 6 bits					
Default	0	0	0	0	0	0	0	0

04h (PWMR2), 05h (PWMG2), 06h (PWMB2)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	PWMx2 6 bits					
Default	0	0	0	0	0	0	0	0

When PWM_ WIDTH =11: 12 bits PWM data is divided into 6 bits and 6 bits data registers for color and luminance data.

The maximum PWM output value will be 63×63 = 3,969.

Table 6 07h Control Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	PWM_WIDTH		-	TSC	SSSET	SSEN
Default	0	0	0	0	0	1	1	0

The PWM_WIDTH is select PWM control mode. When PWM_ WIDTH = 00, the PWM is the traditional 12-bit mode, when PWM_ WIDTH = 01, 10 or 11, the PWM registers are divided into two fields.

An over-temperature protection mechanism is provided to prevent IS32FL3202 from being too hot to burn out the device during operation. When this thermal shut down protection bit (TSC) is enabled, the LED drivers will be shut down when the IS32FL3202 temperature exceeding 165°C.

IS32FL3202 PWM clock can be dithered for improved EMI performance. Clock dithering is achieved by spread spectrum mechanism. Spread spectrum enable bit (SSEN) allows this spread spectrum function enabled or disabled, while SSSET bit can specified the range of clock spread (from 85%-115% with frequency selected at either 200Hz or 5 kHz) when SSEN is enabled.

Due to the principle and mechanism of spread spectrum, and in order to avoid the risk of spread spectrum on LED, If PWM output mode is configured to 16 bits output mode, ±15% 5kHz should to be selected when SSEN is enabled, and ±15% 200Hz only suitable for PWM configuration with 8+8 bits dithering output mode.

PWM_WIDTH	**PWM mode selection**
00	One field PWM mode (Default)
01	Two field PWM mode, PWMx1 = 4 bits and PWMx2 = 8 bits
10	Two field PWM mode, PWMx1 = 5 bits and PWMx2 = 7 bits
11	Two field PWM mode, PWMx1 = 6 bits and PWMx2 = 6 bits

TSC	**Thermal shutdown control**
0	Thermal shutdown Disable
1	Thermal shutdown enable (Default)

SSSET	**Spread spectrum range**
0	±15% 5kHz
1	±15% 200Hz (Only applicable to 8+8 bits dithering output mode)

SSEN	**Spread spectrum function enable**
0	Disable (Default)
1	Enable

Table 7. 08h Control Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	PWMUPD	PFS		-	TCE	PWMMOD	PSM
Default	0	0	0	1	0	0	0	0

When PWMUPD = 0, PWM register content is loaded into PWM operation at the next PWM cycle boundary immediately. When PWMUPD = 1, PWM register content will not be loaded to PWM operation immediately. Only when the host issues a loading special command will the content be loaded into PWM operation at the next PWM

cycle boundary. This can be used when large number of IS32FL3202 is presented in the system, their PWM data can be updated at the same time.

The PFS selects PWM frequency, default is 244Hz.

Temperature Compensation Enable (TCE) is to enable temperature compensation function. This function is described fully previously.

PWMMOD is to define PWM modulation mode. When PWMMOD = 0, PWM modulation is the traditional 16 bits PWM counting method. The PWM frequency (selected by PFS) will be rather low, i.e., 244 Hz when PWM clock is 16MHz. This may cause LED output flickering from the receiving sensor, especially under video camera where it is increasing used in auto interior safety applications. When PWMMOD = 1, an 8-bit+8-bit dithering method is used to make the base PWM frequency up to about 62.4KHz, and the additional PWM width is allocated into 256 PWM cycles. The net visual effect is equivalent to 16 bits PWM method without dithering, but the video flickering can be completely removed.

Power Saving Mode (PSM) allows IS32FL3202 enter low power consumption status and only support enter power saving mode by broadcast command. After entering this mode, PWM output is turned off, system clock switches to a low clock rate, which will not be able to communicate with the system host MCU. The host MCU needs to send a break low (min time 150μs) to wake up the IS32FL3202.

PWMUPD	**PWM update mode**
0	PWM data is latched immediately after PWM data write frame is finished (Default)
1	PWM data is loaded upon receiving special command

PFS	**PWM frequency setting**
00	488Hz
01/11	244Hz (Default)
10	122Hz

TCE	**Temperature compensation enable**
0	Temperature compensation disable (Default)
1	Temperature compensation enable

PWMMOD	**PWM output mode**
0	16 bits output mode (Default)
1	8+8 bits dithering output mode, which is to avoid video flicker effect

PSM	**Power saving mode**
0	Wake up mode (Default)
1	Enter power saving mode (only support broadcast), PWM output is turned off in this mode

After IS32FL3202 enters power saving mode, it can be awakened by a break low signal ≥150μs.

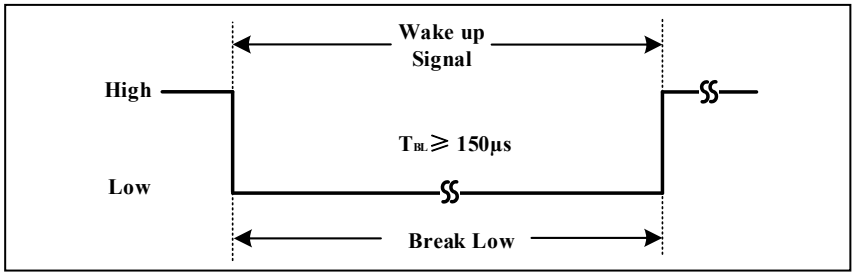


Figure 19 Wake up Signal

Table 8 09h Communication and Command Watchdog Timer Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMDWT_EN	CMDWT_SET			CMTWT_EN	CMTWT_SET		
Default	0	1	0	0	0	1	0	0

Lumibus bus must complete correct operation (read/write/response) within WDT specified time frame. If this WDT timer expired without completion of the operation, a WDTF flag will be set to indicate that there is some communication error. Such scenario could occur, for instance, (1) if when the host is sending a command frame, somehow the frame is corrupted, e.g., due to external RF interference, such that that addressed 3202 cannot receive the complete command frame within a specified time frame, (2) Lumibus host needs to periodically poll status of IS32FL3202 devices and if Lumibus is idled for too long without accessing any IS32FL3202 device, exceeding this specified time frame, this error flag will also be raised. After this flag is raised, the interface state machine is reset to the normal state, ready for the next host communication.

Read Watchdog Timer is used when the host attempts to read IS32FL3202 register. If the read access behaves normally, this Read Watchdog Timer is reset to its initial state, waiting for the next read access command. If, however, after the pre-specified time frame there is still no response, this error flag will be raised and the interface read state machine is reset to the normal state, ready for the next host communication. This could occur, for instance, when the host attempts to read a non-existing device address due to, e.g., a corrupted signal on the Lumibus.

CMTWT_EN	**Communications watchdog timer control**
0	Disable (Default)
1	Enable the communications watchdog timer

CMTWT_SET	**Communications watchdog time selection**
000	8ms
001	16ms
010	32ms
011	64ms
100	128ms (Default)
101	256ms
110	512ms
111	1024ms

CMDWT_EN	**Command watchdog timer control**
0	Disable (Default)
1	Enable the command watchdog timer

CMDWT_SET	**Command watchdog time selection**
000	8ms
001	16ms
010	32ms
011	64ms
100	128ms (Default)
101	256ms
110	512ms
111	1024ms

Table 9 0Ah ADC Control Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ADCCYC_F	ADCCYC_T		ADCCYC	SADC	ADTC		
Default	0	0	0	0	0	0	0	0

The on-die temperature sensor ADC measurement and Red LED VF ADC measurement support cycle sampling and single sampling, and other ADC measurement only support single sampling.

As long as all selected channel measurement are completed and all ADC results are available, the ADCCYC_F bit will be set to “1”, and the ADCCYC_F bit will be clear to “0” when writing the SADC bit to “1” starts the ADC measurement. The ADCCYC_F bit function only for ADC single sampling.

When the on-die ADC is to measure on-die temperature sensor and VF by cycle sampling, it samples once per PWM period for optional 16,32,64 and 128 PWM cycle time (selected by ADCCYC_T) to get the average data. When the ADC is to measure VOUT and VF, the minimum PWM width is limited by the minimum ADC sampling time (depend on ADC measurement frequency and ADC sample hold time, select by 0Bh register). And if VF ADC value is used as reference for temperature compensation, the PWM range of temperature compensation also depend on ADC sampling time, the lower limit of the PWM duty cycle for temperature compensation should be greater than the minimum PWM width is limited of ADC sampling time. When PWM width is less than this minimum sampling time, the result is not counted for that particular PWM period. If the PWM width is shorter than this minimum sampling time for a long period of time, the average reading cannot be finalized. In that case, assuming that this measurement is for temperature compensation, there is no need to perform temperature compensation since the LED temperature is assumed to be low, therefore, there is no need to do any temperature compensation, e.g., lower PWM duty, hence less heat will be generated. And when the PWM modulation is set to the 8 bits+8 bits dithering mode, ADC samples in the 256 dithering periods at the 62.4KHz base PWM cycle, when the ADC is to measure VOUT and VF, the minimum PWM width of each dithering periods is limited by the minimum ADC sampling time (depend on ADC measurement frequency and ADC sample hold time, select by 0Bh register). If the PWM width is shorter than this minimum sampling time for 256 dithering period of time, the ADC result cannot be finalized.

ADTC	**ADC measurement target**
000	On-die temperature sensor (Default)
001	Bandgap
010	VCC
011	OTP pin voltage measurement (measuring range: 0V~1.8V)
100	Red LED VOUT (measuring range: 0V~1.8V)
101	Green LED VOUT (measuring range: 0V~1.8V)
110	Blue LED VOUT (measuring range: 0V~1.8V)
111	Red LED VF (Difference value with power supply and VOUT)

SADC	**Start ADC measurement**
0	ADC measurement stops (Default)
1	ADC measurement starts

Please set ADCEN bit at first, then set SADC bit, otherwise ADC cannot measure voltage.

ADCCYC	**ADC sampling mode**
0	ADC cycle sampling (Default)
1	ADC single sampling

ADCCYC_T	**ADC cycle sampling period**
00	ADC Cycle sampling for 16 PWM cycles (Default)
01	ADC Cycle sampling for 32 PWM cycles
10	ADC Cycle sampling for 64 PWM cycles
11	ADC Cycle sampling for 128 PWM cycles

ADCCYC_F	**Effective reading (only for ADC single sampling)**
0	ADC sampling in progress, ADC result is not valid
1	ADC sampling finished, ADC result is valid reading for host

Table 10 0Bh ADC Enable and Sample Hold Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	ADJEN	ADCEN	ADC_CLK		ADCSH	
Default	0	0	0	0	0	0	0	0

ADJEN **Auto ADC gain and offset adjustment**
0 Disable (Default)
1 Enable

ADC_EN **ADC measurement function enable**
0 Disable (Default)
1 Enable

ADC_CLK **ADC measurement frequency selection**
00 8MHz (Default)
01 4MHz
10 2MHz
11 1MHz
When the ADC measurement target is red LED VF, the ADC measurement frequency should select 2MHz or 1MHz to sampling the VF ADC result.

ADCSH **ADC sample hold time selection**
00 ADC always sampling on (Default)
01 ADC sample time = 2 ADC CLK
10 ADC sample time = 4 ADC CLK
11 ADC sample time = 8 ADC CLK

Table 11 0Ch ADC Measurement Result Register by ADC cycle sampling (ADCR1H, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D11	D10	D9	D8	D7	D6	D5	D4
Default	0	0	0	0	0	0	0	0

Table 12 0Dh ADC Measurement Result Register by ADC cycle sampling (ADCR1L, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	D3	D2	D1	D0
Default	-	-	-	-	0	0	0	0

Store the 12 bits ADC Cycle sampling measurement result of on-die temperature sensor or Red LED VF.
Only on-die temperature sensor ADC measurement and Red LED VF ADC measurement support cycle sampling.

Table 13 0Eh ADC Measurement Result Register ADC single sampling (ADCR2H, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D11	D10	D9	D8	D7	D6	D5	D4
Default	0	0	0	0	0	0	0	0

Table 14 0Fh ADC Measurement Result Register ADC single sampling (ADCR2L, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

ADC single sampling 12 bits ADC measurement result is stored here, all ADC measurement support single sampling.

Table 15 10h Fault Flag Register (Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	WDTF	UV	TSDF	CHKSUMF	-	SHORTF	OPENF
Default	0	0	0	0	0	0	0	0

Fault flag is set to “1” if the corresponding error occurs, which will be cleared after host reads the Fault Flag Register.

OPENF **LED open flag**

0 Normal

1 At least one out of three LEDs is open (Clear after read)

SHORTF **LED short flag**

0 Normal

1 At least one out of three LEDs is short (Clear after read)

0 Normal

CHKSUMF **Checksum error flag; when bandwidth allowed, check this flag after write operation to ensure correct transmission of data**

0 Normal

1 Communication checksum error occurred (Clear after read)

When CRC error occurs, the data of this frame will be invalid, and the host needs to repeatedly issues the data of this frame to devices.

TSDF **Thermal shutdown flag; when fault occurs, current sink is shut off until fault condition is removed**

0 Normal

1 Thermal shutdown occurred (Clear after read)

UV **VCC under-voltage detected**

0 Normal

1 VCC under-voltage occurred 3.5V Typ. (Clear after read)

If the power on time is slower than 110us Typ., the UV flag will be trigger to 1 once, it is recommend reading once for clear during initialization.

WDTF **Watch dog timer time out**

0 Normal

1 Watch dog timer timed out flag

Table 16 11h Open Short Register (Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	STR	STG	STB	-	OPR	OPG	OPB
Default	0	0	0	0	0	0	0	0

Each channel open/short information will be stored at this register, and open/short detection is related to PWM and requires a minimum PWM duty cycle (PWM duty >1% at 16 bits output mode and PWM duty >16% at 8+8 bits dithering output mode) to perform open/short detection.

STx	**LED Short occurred**
xx1 (STR=1)	OUTR Short
x1x (STG=1)	OUTG Short
1xx (STB=1)	OUTB Short

OPx	**LED Open occurred**
xx1 (OPR=1)	OUTR Open
x1x (OPG=1)	OUTG Open
1xx (OPB=1)	OUTB Open

Table 17 12h CRC Error Count

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECRCCNT[7:0]							
Default	0	0	0	0	0	0	0	0

The CRC Error Count default value of is 0 when power-on. When there is a CRC error in a communication frame, ECRCCNT will increase by 1. When it is increased to more than 255, it will remain 255.
If the host writes any value to the CRC Error Count register, the CRC Error Count will be cleared by 0.

Table 18 14h OUTR Output PWM Duty Register (Low 8 bits, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDUTY[7:0]							
Default	0	0	0	0	0	0	0	0

Table 19 15h OUTR Output PWM Duty Register (High 8 bits, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDUTY[15:8]							
Default	0	0	0	0	0	0	0	0

Table 20 16h OUTG Output PWM Duty Register (Low 8 bits, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	GDUTY[7:0]							
Default	0	0	0	0	0	0	0	0

Table 21 17h OUTG Output PWM Duty Register (High 8 bits, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	GDUTY[15:8]							
Default	0	0	0	0	0	0	0	0

Table 22 18h OUTB Output PWM Duty Register (Low 8 bits, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BDUTY[7:0]							
Default	0	0	0	0	0	0	0	0

Table 23 19h OUTB Output PWM Duty Register (High 8 bits, Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BDUTY[15:8]							
Default	0	0	0	0	0	0	0	0

Registers 0x14h-0x19h are the final 16bits PWM output values for OUTR, OUTG, OUTB channel which is used for debugging purpose.

When temperature compensation is disabled, the high 12-bit [15:4] value of registers 0x14h-0x19h is equal to registers 0x01h-0x06h [11:0].

Table 24 1Ch Baud rate Control Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BRMODE	BRCOEF[9:8]		-	-	-	STOPBIT	-
Default	0	0	0	0	0	0	0	0

Table 25 1Dh Baud rate Control Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BRCOEF [7:0]							
Default	0	0	0	0	0	0	0	0

STOPBIT **Stop bit selection**

0: 2 stop bit (Default)

1: 1 stop bit

BRMODE: **Communication baud rate mode setting**

0 Mode1: Configure communication baud rate by Bus reset SYNC (Default)

1 Mode2: Configure communication baud rate by BRCOEF[9:0]

The communication baud rate of IS32FL3202 supports two modes: mode 1 is to directly use the Bus reset signal SYNC frequency to set the communication baud rate; mode 2 is to send SYNC with 100kbps baud rate, and then reconfigure the required baud rate by Baud rate Control Register(1Ch/1Dh). It is recommended to use mode 2 to set the baud rate to when multiple applications are cascaded.

BRCOEF[9:0]: 10-bit baud rate setting register

BRCOEF [9:0] = 1024/(target baud rate /100k)

Example:

Target baud rate is 2Mbps:

BRCOEF [9:0] = 1024/(2000k/100k) = 1024/20 = 51(DEC)

Target baud rate is 500Kbps:

BRCOEF [9:0] = 1024/(500k/100k) = 1024/5 = 205(DEC)

Table 26 40h OTP Status Register (Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	2Err_ecc_all	1Err_ecc_all	FAIL	FINISH	BUSY
Default	0	0	0	0	0	0	1	0

Table 27 41h ECC Status Register 1 (Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	1Err_eccE	1Err_ecc D	1Err_ecc C	-	-
Default	0	0	0	0	0	0	0	0

Table 28 42h ECC Status Register 2 (Read Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	2Err_eccE	2Err_ecc D	2Err_ecc C	-	-
Default	0	0	0	0	0	0	0	0

1Err_ecc_all At least one of zone ECC detected 1bit error
2Err_ecc_all At least one of zone ECC detected 2bits error
FAIL OTP write fail
FINISH OTP write finish
BUSY OTP operation in progress
1Err_eccX ECC detected 1bit error in zone X (X= C, D, E)
2Err_eccX ECC detected 2bits error in zone X (X= C, D, E)

OTP Content Registers

Table 29 29h~2Fh Temperature Compensation Configuration Register

29h OTPCRC0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Kval[1:0]		N_R1[5:0]					
Default	0	0	0	0	0	0	0	0

2Ah OTPCRC1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_R2[5:0]						N_R3[5:4]	
Default	0	0	0	0	0	0	0	0

2Bh OTPCRC2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_R3[3:0]				N_G1[5:2]			
Default	0	0	0	0	0	0	0	0

2Ch OTPCRC3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_G1[1:0]		N_G2[5:0]					
Default	0	0	0	0	0	0	0	0

2Dh OTPCRC4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_G3[5:0]						N_B1[5:4]	
Default	0	0	0	0	0	0	0	0

2Eh OTPCRC5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_B1[3:0]				N_B2[5:2]			
Default	0	0	0	0	0	0	0	0

2Fh OTPCRC6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_B2[1:0]		N_B3[5:0]					
Default	0	0	0	0	0	0	0	0

Kval: Temperature Compensation Steps (00=8°C, 01=2°C, 10=4°C, 11=16°C)

N_R/G/B 1: Red/Green/Blue LED channels temperature compensation percentage at -40°C ~15°C

N_R/G/B 2: Red/Green/Blue LED channels temperature compensation percentage at -16°C ~70°C

N_R/G/B 3: Red/Green/Blue LED channels temperature compensation percentage at -71°C ~125°C

Table 30 30h~32h OUTR/G/B Channels Output Current and VF Reference register

30h OTPCRC7

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R_DC[5:0]						G_DC[5:4]	
Default	0	0	0	0	0	0	0	0

31h OTPCRC8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	G_DC[3:0]				B_DC[5:2]			
Default	0	0	0	0	0	0	0	0

32h OTPCRC9

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	B_DC[1:0]		VF_Ref[5:0]					
Default	0	0	0	0	0	0	0	0

R/G/B_DC [5:0]: DC register for OUTx, control the DC output current of each channel. Each channel has 6bit data to modulate DC current in 64 steps.

VF_Ref [5:0]: Red LED VF ADC measurement value trim register.

Table 31 33h OTPCRC10 VF ADC value at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	T_ADC_F[7:0]							
Default	0	0	0	0	0	0	0	0

T_ADC_F [7:0]: Store VF ADC measurement value at Room Temperature.

Table 32 34h OTPCRC11 ECC Data of C Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECC_C[7:0]							
Default	0	0	0	0	0	0	0	0

ECC_C: ECC data of C zone

Table 33 35h OTPCRC12 Protect bit of C Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_C	-						
Default	0	0	0	0	0	0	0	0

PT_C: protection bit of C zone

Table 34 36h~3Bh OUTR/G/B PWM Output Calibration Register

36h OTPCRD0 OUTR PWM Output Calibration Register (Low 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R_PWM_CAL[7:0]							
Default	0	0	0	0	0	0	0	0

37h OTPCRD1 OUTR PWM Output Calibration Register (High 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R_PWM_CAL[15:8]							
Default	0	0	0	0	0	0	0	0

38h OTPCRD2 OUTG PWM Output Calibration Register (Low 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	G_PWM_CAL[7:0]							
Default	0	0	0	0	0	0	0	0

39h OTPCRD3 OUTG PWM Output Calibration Register (High 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	G_PWM_CAL[15:8]							
Default	0	0	0	0	0	0	0	0

3Ah OTPCRD4 OUTB PWM Output Calibration Register (Low 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	B_PWM_CAL[7:0]							
Default	0	0	0	0	0	0	0	0

3Bh OTPCRD5 OUTB PWM Output Calibration Register (High 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	B_PWM_CAL[15:8]							
Default	0	0	0	0	0	0	0	0

Table 35 3Ch OTPRCD6 ECC Date and Protection bit of D Zone

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_D	ECCD[6:0]						
Default	0	0	0	0	0	0	0	0

ECC_D: ECC data of D zone

PT_D: protection bit of D zone

Table 36 3Dh OTPCRE0 NAD Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SNPD NAD[7:0]							
Default	0	0	0	0	0	0	0	0

SNPN_NAD: store NAD (device address)

Table 37 3Eh OTPCRE1 ECC data of E Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECC_E[7:0]							
Default	0	0	0	0	0	0	0	0

ECC_E: ECC data of E zone

Table 38 3Fh OTPCRE2 Protection bit of E Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_E	-						
Default	0	0	0	0	0	0	0	0

PT_E: protection bit of E zone

OTP NVM Registers

Table 39 69h~6Fh Temperature Compensation Configuration Register

69h OTPNRC0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Kval[1:0]		N_R1[5:0]					
Default	0	0	0	0	0	0	0	0

6Ah OTPNRC1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_R2[5:0]						N_R3[5:4]	
Default	0	0	0	0	0	0	0	0

6Bh OTPNRC2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_R3[3:0]				N_G1[5:2]			
Default	0	0	0	0	0	0	0	0

6Ch OTPNRC3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_G1[1:0]		N_G2[5:0]					
Default	0	0	0	0	0	0	0	0

6Dh OTPNRC4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_G3[5:0]						N_B1[5:4]	
Default	0	0	0	0	0	0	0	0

6Eh OTPNRC5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_B1[3:0]				N_B2[5:2]			
Default	0	0	0	0	0	0	0	0

6Fh OTPNRC6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_B2[1:0]		N_B3[5:0]					
Default	0	0	0	0	0	0	0	0

Kval: Temperature Compensation Steps (00=8°C, 01=2°C, 10=4°C, 11=16°C)

N_R/G/B 1: Red/Green/Blue LED channels temperature compensation percentage at -40°C ~15°C
N_R/G/B 2: Red/Green/Blue LED channels temperature compensation percentage at -16°C ~70°C
N_R/G/B 3: Red/Green/Blue LED channels temperature compensation percentage at -71°C ~125°C

Table 40 70h~72h OUTR/G/B Channels Output Current and VF Reference register

70h OTPNRC7

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R_DC[5:0]						G_DC[5:4]	
Default	0	0	0	0	0	0	0	0

71h OTPNRC8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	G_DC[3:0]				B_DC[5:2]			
Default	0	0	0	0	0	0	0	0

72h OTPNRC9

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	B_DC[1:0]		VF_Ref[5:0]					
Default	0	0	0	0	0	0	0	0

R/G/B_DC [5:0]: DC register for OUTx, control the DC output current of each channel. Each channel has 6bit data to modulate DC current in 64 steps.

VF_Ref [5:0]: Red LED VF ADC measurement value trim register.

Table 41 73h OTPNRC10 VF ADC value at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	T_ADC_F[7:0]							
Default	0	0	0	0	0	0	0	0

T_ADC_F [7:0]: Store VF ADC measurement value at Room Temperature.

Table 42 74h OTPNRC11 ECC Data of C Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECC_C[7:0]							
Default	0	0	0	0	0	0	0	0

ECC_C: ECC data of C zone

Table 43 75h OTPNRC12 Protect C Protect bit of C Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_C	-						
Default	0	0	0	0	0	0	0	0

PT_C: protection bit of C zone

Table 44 76h~7Bh OUTR/G/B PWM Output Calibration Register

76h OTPNRD0 OUTR PWM Output Calibration Register (Low 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R_PWM_CAL[7:0]							
Default	0	0	0	0	0	0	0	0

77h OTPNRD1 OUTR PWM Output Calibration Register (High 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R_PWM_CAL[15:8]							
Default	0	0	0	0	0	0	0	0

78h OTPNRD2 OUTG PWM Output Calibration Register (Low 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	G_PWM_CAL[7:0]							
Default	0	0	0	0	0	0	0	0

79h OTPNRD3 OUTG PWM Output Calibration Register (High 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	G_PWM_CAL[15:8]							
Default	0	0	0	0	0	0	0	0

7Ah OTPNRD4 OUTB PWM Output Calibration Register (Low 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	B_PWM_CAL[7:0]							
Default	0	0	0	0	0	0	0	0

7Bh OTPNRD5 OUTB PWM Output Calibration Register (High 8bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	B_PWM_CAL[15:8]							
Default	0	0	0	0	0	0	0	0

Table 45 7Ch OTPNRD6 ECC Date and Protection bit of D Zone

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_D	ECC_D[6:0]						
Default	0	0	0	0	0	0	0	0

ECC_D: ECC data of D zone

PT_D: protection bit of D zone

Table 46 7Dh OTPNRE0 NAD Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SNPD NAD[7:0]							
Default	0	0	0	0	0	0	0	0

SNPN_NAD: store NAD (device address) on OTP

Table 47 7Eh OTPNRE1 ECC data of E Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	EccE[7:0]							
Default	0	0	0	0	0	0	0	0

ECC_E: ECC data of E zone

Table 48 7Fh OTPNRE2 Protection bit of E Zone Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_E	-						
Default	0	0	0	0	0	0	0	0

PT_E: protection bit of E zone

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

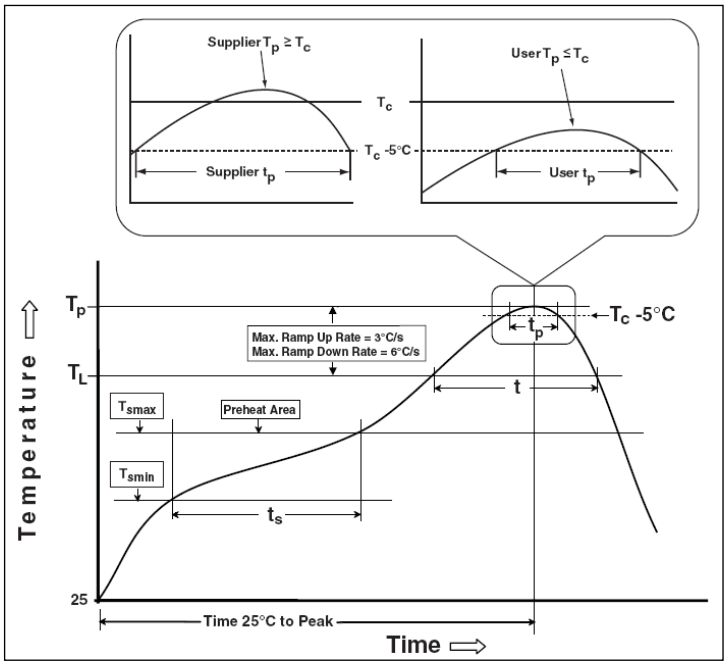
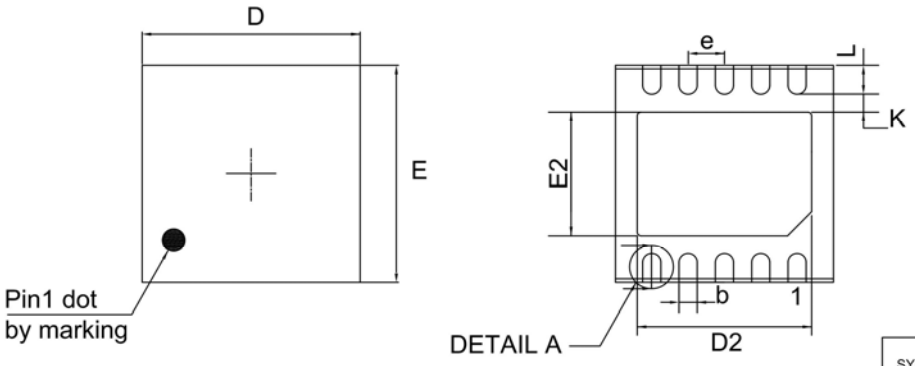
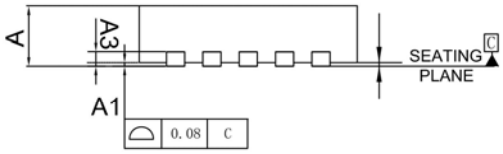


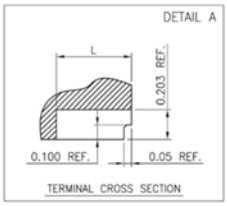
Figure 22 Classification Profile

PACKAGE INFORMATION

WFDFN-10







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3		0.20REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E2	1.55	1.65	1.70
D2	2.20	2.30	2.35
b	0.18	0.25	0.30
L	0.30	0.40	0.50
K	0.20	—	—
e		0.50 BSC	

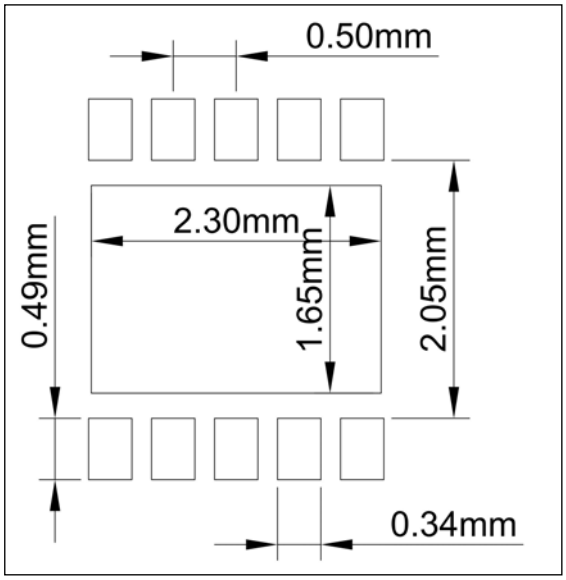
233-570-410 Rev.A

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-229F
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES

RECOMMENDED LAND PATTERN

WFDFN-10



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2023.09.08
A	Update to final version	2023.12.26