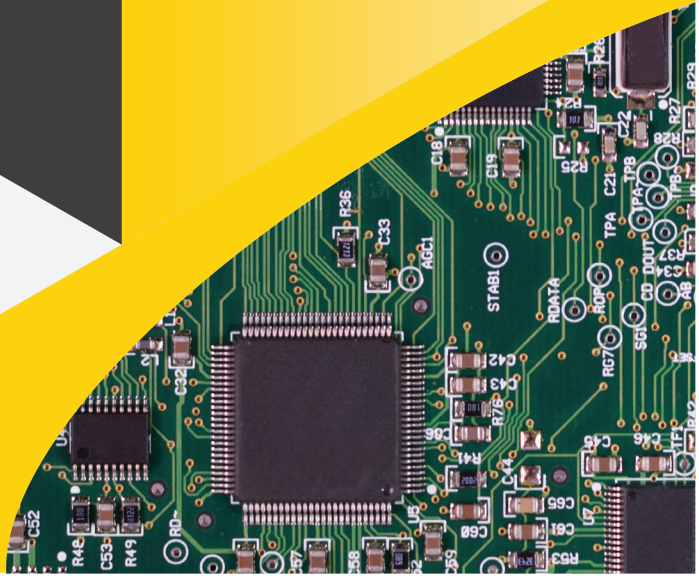
LUMISSIL MICROSYSTEMS

32-Bit Multi-Core MPU Family for Multimedia and Real-Time Control



This article introduces two 32-bit Multi-Core Families that expand on Lumissil's Multiprocessor (MPU) portfolio: the X1600 and X2000. These MPUs utilize XBurst, a family of MIPS processors with (FPU) Floating Point Unit, dedicated security processor and use a System-in-Package (SIP) architecture to house memory. These features facilitate complex DSP computations, enable authentication, perform encryption/decryption and manage data storage. By integrating these features, the need for costly licenses is eliminated, simplifying design and reducing the BOM cost typically associated with competing in-class MPUs.

For compute-intensive applications, the X2000 Multi-Core MPU family features XBurst0, a CPU running at 1.2GHz. This processor supports both single and dual-core configurations and offers options for high-performance or low-power modes. These MPUs enable embedded engineers to design systems that efficiently execute instructions, process data, and perform real-time tasks simultaneously, making them ideal for demanding applications that require both speed and adaptability.

For cost-sensitive applications, the X1600 Multi-Core MPU family features the XBurst1 processor. Operating at speeds up to 1.0 GHz, XBurst1 provides an efficient and economical solution without compromising on essential performance.

The X1600 is found in barcode/QR code readers, printers, and RFID equipment, where it performs scan and print functions as well as storage of information.

As an example, how do MPUs function in code scanners and checkout kiosks? In code scanners, MPUs decode barcode/QR code and facilitate data storage and retrieval. In checkout kiosks, MPUs manages a range of functions: they process scanned barcodes, handle payment transactions and print receipts. Additionally, in advanced systems, MPUs control cameras to capture customers' photos for verification purposes.

In summary, Lumissil MPUs are perfect for both cost sensitive and compute intensive applications.

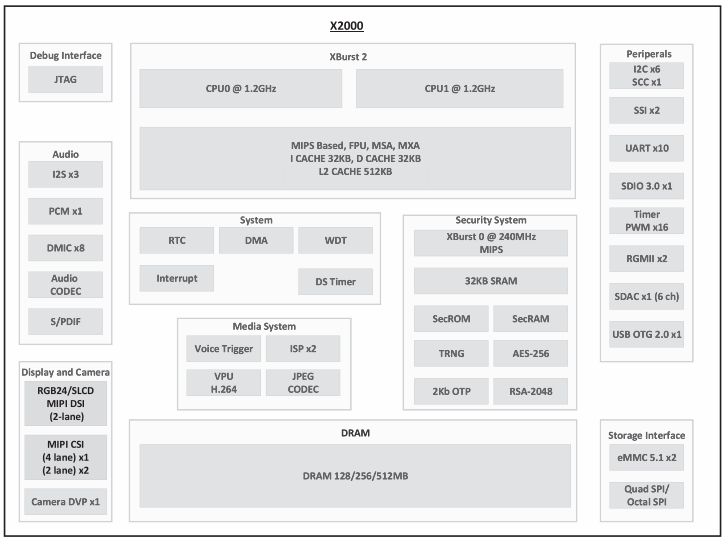


Figure 1: Block Diagram

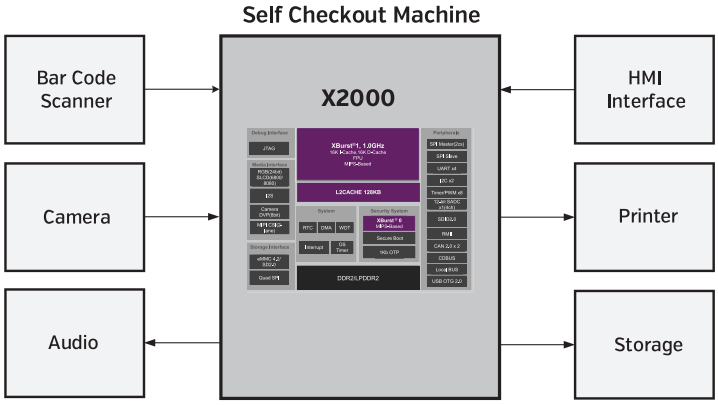


Figure 2: Self-Service Checkout System

KEY ADVANTAGES AND BENEFITS INCLUDE:

ReconfigurableSingle/Dual Core CPU: Supports simultaneously real-time execution and processing of commands through a single or dual core architecture. This architecture allows for tailored performance while enhancing responsiveness. This reconfigurable design allows for scalability in performance, making it suitable for a wider range of applications.

Reconfigurable High Performance/Power Savings CPU Modes: Reconfigurable CPUs with high-performance and power savings modes offer significant advantages. This dual-mode capability allows the CPU to dynamically switch between high-performance and energy-efficient modes based on current workload demands. In high-performance mode, the CPU delivers maximum processing power, handling intensive tasks and applications with ease. Conversely, in power savings mode, the CPU optimizes energy consumption and reduces operational costs. This adaptability enhances system responsiveness and efficiency while promoting sustainability and cost-effectiveness, making the CPU versatile for both demanding and resource-constrained applications.

Dedicated Security CPU: A dedicated security CPU offers robust protection for sensitive information with advanced encryption and decryption capabilities. By independently handling cryptographic operations, it enhances the efficiency and effectiveness of data protection while minimizing the performance impact on the main CPU. Additionally, integrated security memory further strengthens protection by securely storing cryptographic keys and sensitive data, reducing the risk of data breaches and unauthorized access. These features provide a comprehensive security solution, making dedicated security CPUs ideal for applications requiring high levels of data confidentiality and integrity.

On-board Memory: On-board memory offers significant benefits for both system performance and efficiency. By integrating memory directly, latency associated with data transfers between the processor and external memory is minimized, resulting in faster data access and improved overall system responsiveness. Integrated memory reduces the need for external memory modules, which simplify design and reduce BOM costs.

Floating Point Unit (FPU): An integrated FPU offers substantial benefits by eliminating costly licensing fees often associated with competing in-class MPUs. By incorporating the FPU directly into the CPU, systems achieve more efficient and cost-effective floating-point computations, crucial for tasks involving complex mathematical calculations, such as video processing and file compression. This integration not only reduces overall system costs but simplifies the design and development process, as there is no need to source and integrate separate FPU components. Additionally, having an on-chip FPU enhances processing speed and performance by enabling faster execution of floating-point operations, leading to smoother and more responsive applications.

Camera ISP and CODEC: Camera ISP (Image Signal Processor) and CODEC (Coder-Decoder) together deliver substantial benefits for image and video processing systems. ISPs enhance image quality by performing noise reduction, color correction, and detail enhancement, ensuring that captured images are clear, vibrant, and true. It optimizes the raw sensor data to produce high-quality visuals, crucial for high end surveillance systems. The integrated CODEC, on the other hand, efficiently compresses and decompresses video streams, reducing file sizes and bandwidth requirements while maintaining video quality. This dual integration enables real-time streaming and recording of high-definition video with minimal latency and storage overhead.

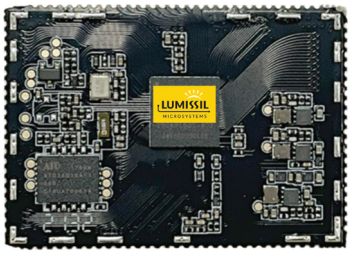
Wide Range of Peripheral Interface: These MPUs feature a wide range of interfaces ranging from JTAG to communications, to display and to camera interfaces such as MIPI-DSI and MIPI-CSI for flexibility and scalability.

COMMON USES CASES OF THE FAMILY INCLUDE:

1. **Bar code readers:** Reads, decodes, processes and stores bar code information.
2. **Credit card processing units:** Reads, processes, and transmits/receives secure information and prints receipts.
3. **Industrial control systems:** Monitors, records, process, controls and stores critical information.
4. **Network equipment:** Transmits/receives and stores data frames securely.
5. **Surveillance equipment:** Records, encrypt and stores video/audio streams.
6. **Smart TV controllers:** Accepts and processes TV commands from IR controllers.
7. **Camera equipment:** Processes recorded photo images and control settings and records and stores images on to external memory drives.
8. **Media players:** Accepts command information from a push interface, provides control functions, and decrypts video/audio data streams.

DEVELOPMENT KIT

Lumissil makes developing MPU applications easy with Halley 5 and Halley 6, which are application kits for the X2000 and X1600 respectively. As a bonus, the application kits are designed around X2000 and X1600 modules to ease design and facilitate faster time to market. Lumissil offers a growing family of MPUs with advanced capabilities to support modern systems by increasing system performance accelerating time to market while decreasing BOM cost.



X2000 Module

Halley 5

TABLE 2: X2000 MULTI-MPU FAMILY

Part	Description	Availability
X2000	Multi-Core MPU with 128MB LPDDR3	Now
X2000E	Multi-Core MPU with 256MB LPDDR2	Now
X2000H	Multi-Core MPU with 512MB LPDDR3	Now

TABLE 3: X1600 MULTI-MPU FAMILY

Part	Description	Availability
X1600	Multi-Core MPU featuring XBurst1 and 32MB LPDDR2	Now
X1600E	Multi-Core MPU featuring XBurst1 and 64MB LPDDR2	Now
X1600HN	Multi-Core MPU featuring XBurst1 and 128MB DDR2	Now

KEY FEATURES

Features	X2000 Family	X1600 Family
Main Processor	XBurst0 @ 1.2GHz • Reconfigurable as a single or dual core CPU • Features a high performance and low power mode	XBurst1 @ 1GHz
Security Processor & Memory	XBurst2 @ 240MHz 32KB	XBurst0 @ 240MHz -
Main Memory	128MB LPDDR3 256MB LPDDR2 512MB LPDDR3	32MB LPDDR2 64MB LPDDR2 128MB LPDDR2
L1 and L2 Cache	L1: 32KB I/D Cache L2: 512KB Cache	L1: 16K I/D Cache L2: 128KB Cache
FPU	Yes	Same
Camera Interface	DVP, MIPI-CSI	Same
Storage Interface	MMC, SD, SDIO	Same
Debug Interface	JTAG	Same
Display Interface	SLCD, RGB MIPI-DSI	Same -
Package	BGA-270	BGA-159